TEXAS INSTRUMENTS

Digital Logic

Pocket Data Book

2003 SLL

Digital Logic

Pocket Data Book

TEXAS INSTRUMENTS

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Little Logic

Series	Supply Voltage Vcc (V)	Operating Free-air Temperature Ta (°C)
SN74AUC1G/2G/3G	0.8～2.7	–40～85
SN74LVC1G/2G/3G	1.65～5.5	–40～85
SN74AHC1G	2.0～5.5	–40～85
SN74AHC1GxxH	2.0～5.5	–40～85
SN74AHC2GxxH	2.0～5.5	–40～85
SN74AHCT1G	4.5～5.5	–40～85

GATE/OCTAL/Widebus™/Widebus+

Series	Supply Voltage Vcc (V)	Operating Free-air Temperature Ta (°C)
SN74ABT	4.5～5.5	–40～85
SN74BCT SN74F SN74ALS SN74AS	4.5～5.5	0～70
SN74LS SN74S SN74xx(STD)	4.75～5.25	0～70
SN74AC SN74AC11 SN74AHC	2.0～5.5	–40～85
SN74HC	2.0～6.0	–40～85
SN74LV	2.0～5.5	–40～85
SN74LVC	2.0～3.6	–40～85
SN74LVT	2.7～3.6	–40～85
SN74ALVC	1.65～3.6	–40～85
SN74ALVT	2.3～3.6	–40～85
SN74AVC	1.4～3.6	–40～85

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Production processing does not necessarily include testing of all parameters.
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FUNCTION

GATE (AND/NAND/OR/NOR)

Description	No. of Input	Curcuit	Input	Output	Device	Technology: Bipolar TTL	LS	S	ALS	AS	F	CMOS HC	HCT	BiCMOS BCT	ABT	LVT	ALVT	Advanced CMOS AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
POS-AND	2	4			08	×	○	○	○	○	○	○/○	○/○					○/○/○	○/○/○	○	○	○A	○A	○	
				OC	09	×	○	○	○		×	×/-													
				OC	15		×	×	×																
				BUF	1008				×A	○A															
			SCH		7001							○/-													
		6		BUF	808				×	○B		×/-													
				BUF	1808				×	×															
	3	3			11		○	×	○A	○	○	○/○	-/○					×/○/-	×/○/-			○A			
				BUF	1011				×																
	4	2			21		○		○A	○	○	○/○	×/○					×/-/-	×/-/-			○A			
POS-NAND	2	2			8003				×	○															
		4			00	○	○	○	○A	○	○	○/○	○/○					○/○/○	○/○/○	○	○	○A	○A	○	
				OC	01	×	×		×			×/-													
				OC	03	×	○	×	○B			○/○	-/○												
			SCH		24		×																		
				OC	26	×	○																		
				BUF	37	×	○	○	○A		×														
				OC	38	○	○	○	○B		○														
			SCH		132	×	○	×				○/○	-/○					×/-/-	×/-/-	○	○	○A			
				BUF	1000				×A	○A															
				OC	1003				×A																
			SCH	OC	7003						×	×/-													
				OC	39	×																			
		6		BUF	804				○A	○B		×/-													
				BUF	1804				×A	×															
	3	3			10	○	○	○	○A	○	○	○/○	-/○					×/○/○	×/○/○			○A	○A	○	
				OC	12	×	×		×																
				BUF	1010				×																
		2	SCH		13	×	×											×/-/-	-/×/-						
			SCH		18		×																		
	4				20	×	○	×	○A	○	○	○/○	-/○					×/×/○	×/×/○			○A			
				OC	22	×	×	×	×																
				BUF	40	×	×	×	×		×														
				BUF	140			○																	
				BUF	1020				×																
		3	SCH		618		×																		
	8	1			30	×	○	×	○A	○	○	×/○	-/○					×/-/×	○/-/×						
	12	1		3S	134			×																	
	13	1			133			×	○			×/-													
POS- OR	2	4			32	○	○	○	○	○	○	○/○	○/○					○/○/○	○/○/○	○	○	○A	○A	○	
				BUF	1032				×	○A															
			SCH		7032							○/-													
		6		BUF	832				○A	○B		×/-													
				BUF	1832				×A	×															
	3	3			4075							×/○	-/○												
POS- NOR	2	4			02	○	○	○	○A	○	○	○/○	○/○					×/-/○	×/-/○	○	○	○A	○A		
				BUF	28	×	×		×																
				OC	33	×	○		○A																
					36						×	×/-													
				BUF	128	○																			
				BUF	1002				×A																
			SCH		7002							○/-													
				BUF	1036					×A															
		6		BUF	805				○A	○B		×/-													
				BUF	1805				×	×															
	3	3			27	×	○		○A	○	○	○/○	-/○					×/-/×	×/-/×			○A			
	4	2			23	×																			
					25	○																			
					4002							×/○													
	5	2			260			○			○														

Explanatory notes [Input] SCH : Schmitt-Trigger Inputs

[Output] BUF : Buffered Output OC : Open-Collector Output 3S : 3-State Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated

× : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

GATE (EX-OR/EX-NOR/INVERTER/NONINVERTER/etc.)

Description	No. of Input	Curcuit	Input	Output	Device	Technology: Bipolar TTL	Bipolar LS	Bipolar S	Bipolar ALS	Bipolar AS	Bipolar F	CMOS HC	CMOS HCT	BiCMOS BCT	BiCMOS ABT	BiCMOS LVT	BiCMOS ALVT	Advanced CMOS AC	Advanced CMOS ACT	Advanced CMOS AHC	Advanced CMOS AHCT	Advanced CMOS LV	Advanced CMOS LVC	Advanced CMOS ALVC	Advanced CMOS AVC
EX-OR	2	4			86	×	○A	○	○	○A	○	○/○	-/○					○/○/○	×/○/○	○	○	○A	○A		
				OC	136	×	○		×	×															
					386		×					×/-													
EX-NOR	2	4		OC	266		○					○/-													
					810				×	×								×/-/-	×/-/-						
				OC	811				×	×															
					7266							×/○													
EX-OR/NOR	2	4			135			×																	
INVERTING	1	6			04	○	○	○	○B	○	○	○/○	○/○					○/○/○	○/○/○	○	○	○A	○A	○	
				OC	05	×	○	○	○A			○/-						-/-/○	-/-/○	○		○A			
				OC	06	○	○															○A	○A		
			SCH		14	○	○					○/○	○/○					×/○/○	×/○/○	○	○	○A	○A	○	
				OC	16	○																			
			SCH		19		○A																		
				BUF	1004				○	○A															
				OC	1005				○																
					4049							—/○													
					U04							○/○								○		○A	○A		
		8	SCH		619		×																		
NON-INVERTING	1	4			425	×																			
					426	×																			
		6		OC	07	○	○															○A	○A		
				OC	17	○																			
					34				×	×								×/-/-	×/-/-						
				OC	35				○A																
				BUF	1034				○	○A															
				OC	1035				○																
					4050							—/○													
OTHER	1	6			63		×																		
	2	6			31		○																		
	4	2			50	×																			
					51	×	○	×			×	×/-						×/-/-	×/-/-						
					60	×																			
	8	1			53	×																			
					55		×																		
					4078							×/-													
	10	1			54	×	×																		
	11	1			64			×			×							×/-/-	×/-/-						
				OC	65			×																	
	12	3		BUF	800													×/-/-	×/-/-						
				BUF	802													×/-/-	×/-/-						
	-	6			7006							×/-													
					7008							×/-													
					7074							×/-													
					7075							×/-													
					7076							×/-													

Explanatory notes [Input] SCH : Schmitt-Trigger Inputs

[Output] BUF : Buffered Output OC : Open-Collector Output 3S : 3-State Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated

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HC : SN74HCxx / CD74HCxx

HCT : SN74HCxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUFFER/DRIVER(NON-INVERTING)

Description	No. of Output	Output	Device	Technology: Bipolar TTL	Bipolar LS	Bipolar S	Bipolar ALS	Bipolar AS	Bipolar F	CMOS HC	CMOS HCT	BiCMOS BCT	BiCMOS ABT	BiCMOS LVT	BiCMOS ALVT	Advanced CMOS AC	Advanced CMOS ACT	Advanced CMOS AHC	Advanced CMOS AHCT	Advanced CMOS LV	Advanced CMOS LVC	Advanced CMOS ALVC	Advanced CMOS AVC
NON-INVERTING	4	3S	125	×	○A			○	○	○/○	○/○	○A/○A	○	H○				○	○	○A	○A	○	
		3S	126	×	○A			○	○	○/○	-/○	×A/○A	○	H○				○	○	○A	○A	○	
	6	3S	365	×	○A					○/○	-/○												
		3S	367	×	○A					○/○	-/○							○	○	○A			
	8	3S	241		○	○	○C	○A	○	○/○	×/○	○/-	○A	H○		×/○/-	×/○/○				-		
		3S	244		○	○	○C/ ○C1	○A	○	○/○	○/○	○/○	○A	○B/ T○/ H○A/ Z○		○/○/○	○/○/○	○	○	○A	○A/ H○A/ Z○A	○/H○	
		3S	455									×/-											
		3S	465	○			×																
		3S	467	×			×																
		3S	541		○		○/○1		○	○/○	○/○	○A/-	○B	H○		-/-/○	-/-/○	○	○	○A	○A		
		3S	656													×/-/-	×/-/-						
		3S	747				×																
		OC	757					○				○/○											
		OC	760				○	○				○/-											
		3S	1241																				
		3S	1244				○A																
		R3S	2241									○/-	○										
		R3S	2244					×				○/-	○A								○A		
		R3S	2541				○																
		3S	25241									×/-											
		3S	25244									○/○											
		OC	25757									×/-											
		OC	25760									×/-											
	10	3S	827										○			×/-/-	×/-/-				○A		
		R3S	2827									○C/-	○										
		3S	29827				○					○B/-											
	11	R3S	5400										○A										
	12	3S	5402										○A										
		R3S	16903																			H○	
	16	3S	16241										○A	H○			×				H×A		
		3S	16244										○A/ H○	○B/ H○A	H○	○	○	○	○		○A/ H○A/ Z○A	○A/ H○	○
		3S	16541										○A	H○			○	○	○		H○A	×	
		R3S	162241											H○									
		R3S	162244										○	○A/H○	H○						○A/ H○A	H○	
		R3S	162541											H○								×	
	18	3S	16825										○				○					H○	
		R3S	162825										○										
		3S	16835											H○								○/ H○	○
		R3S	162835																			○/ H○	
	20	3S	16827										○		H○		○					H○	○
		3S	162827										○A		H○							H○	
	32	3S	32244											○/H○	H○						○/H○	H○	

Explanatory notes [Output] 3S : 3-State Output R3S : Series Resistor and 3-State Output OC : Open-Collector Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated

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ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUFFER/DRIVER(INVERTING,INVERTING AND NON-INVERTING,ADDRESS DRIVERS)

Description	No. of Output	Output	Device	Technology: Bipolar TTL	LS	S	ALS	AS	F	CMOS HC	HCT	BiCMOS BCT	ABT	LVT	ALVT	Advanced CMOS AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
INVERTING	6	3S	366	×	×					×/○													
		3S	368	×	○A					○/○	-/○												
		3S	436			×																	
		3S	437	×																			
	8	3S	231				×	×															
		3S	240		○	○	○A/○A1	○A	○	○/○	○/○	○/-	○A	○A/H○		○/○/○	○/○/○	○	○	○A	○A/Z○A		
		3S	456									×/-											
		3S	466		×		×																
		3S	468		×		×																
		3S	540		○		○/○1		×	○/○	○/○	○A/-	○	H○		-/-/○	-/-/○	○	○	○A	○A		
		3S	655													×/-/-	×/-/-						
		3S	746				×																
		OC	756				×	○				○/-											
		OC	763					×															
		3S	1240				×																
		R3S	2240				×					○/-	○A										
		R3S	2540				×																
		3S	25240									×/-											
		OC	25756									×/-											
	10	3S	828													×/-/-	×/-/-				○A		
		R3S	2828									×/-											
		3S	29828				■					×B/-											
	11	R3S	5401										○										
	12	R3S	5403										○										
	16	3S	16240										○A	○/H○	H○	×	○	○	○		H○A/Z○A	H○	
		3S	16540										○A				×	○	○		H○A	×	
		R3S	162240											○/H○								-	
		R3S	162540																			×	
	20	3S	16828														×					×	
	32	3S	32240											○									

Description	No. of Output	Output	Device	Technology: Bipolar TTL	LS	S	ALS	AS	F	CMOS HC	HCT	BiCMOS BCT	ABT	LVT	ALVT	Advanced CMOS AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
INVERTING AND NON-INVERTING	8	3S	230				×	×															
		OC	762					×															

Description	No. of Output	Output	Device	Technology: Bipolar TTL	LS	S	ALS	AS	F	CMOS HC	HCT	BiCMOS BCT	ABT	LVT	ALVT	Advanced CMOS AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
ADDRESS DRIVERS	1-2	3S	16830																			H*	
		R3S	162830																			H○/HS○	
	1-4	3S	16344																			H○	
		3S	16831																			H○	
		3S	16832																			H○	
		R3S	162344																			H○	
		R3S	162831																			○/H○	
		R3S	162832																			H○	

Explanatory notes [Output] 3S : 3-State Output R3S : Series Resistor and 3-State Output OC : Open-Collector Output

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ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

J/K FLIP-FLOP

Trigger	Curcuit	PRE・CLR	Output	Q・/Q	Device	Technology: Bipolar TTL	LS	S	ALS	AS	F	CMOS HC	HCT	BiCMOS BCT	ABT	LVT	ALVT	Advanced CMOS AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
POS	1	B	2S	B	72	×																			
	2	B	2S	B	70	×																			
		B	2S	B	73	×	○A					×/○	-/○												
		B	2S	B	109	×	○A		○A	○A	○	○/○	-/○					×/-/○	×/-/○						
		B	2S	B	110	×																			
		B	2S	B	111	×																			
	4	B	2S	Q	376	×																			
NEG	2	B	2S	B	76	×	×					×/-													
		B	2S	B	78		×					×/-													
		B	2S	B	107	○	○A					×/○	-/○												
		B	2S	B	112		○A	○A	○A		○	○/○	-/○					×/-/○	×/-/○				○A		
		B	2S	B	113		×	×	×		×	×/-													
		B	2S	B	114		×	×	×		×	×/-													
	4	B	2S	Q	276	×																			

D-TYPE FLIP-FLOP

Trigger	Curcuit	PRE・CLR	Output	Q・/Q	Device	Technology: Bipolar TTL	LS	S	ALS	AS	F	CMOS HC	HCT	BiCMOS BCT	ABT	LVT	ALVT	Advanced CMOS AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
POS	2	B	2S	B	74	×	○A	○	○A	○A	○	○/○	○/○					○/○/○	○/○/○	○	○	○A	○A		
	4	C	2S	B	171		×																		
		C	2S	B	175	×	○	○	○	○B	○	○/○	-/○					○/-/○	×/-/○			○A			
			2S	B	379		×				×	×/-						×/-/-	×/-/-						
	6	C	2S	Q	174	×	○	○	○	○	○A	○/○	-/○					×/-/○	×/-/○	○	○	○A			
			2S	Q	378		○				×	×/-						×/-/-	×/-/-						
	8	C	2S	Q	273	×	○		○		×	○/○	○/○		○	H○		×/-/○	×/-/○	○	○	○A			
			3S	Q	374		○	○	○A	○	○	○/○	○/○	○/-	○A	H○		×/○/○	○/○/○	○	○	○A	○A	H○	
			2S	Q	377		○			○A	○	○/○	○/○		○A			×/-/-	×/-/-						
			3S	Q	478													×/-/-	×/-/-						
			3S	/Q	534				○A	×	×	×/○	×/○	×/-	○A			×/○/○	×/○/-						
			3S	/Q	564				○B		×	×/○	×/○	×/-				×/○/-	×/○/-						
			3S	Q	574				○B	○	○	○/○	○/○	○/-	○A	H○		×/○/○	×/○/○	○	○	○A	○A		
			3S	Q	575				○A	×															
			3S	/Q	576				○B	○															
			3S	/Q	577				○A	×															
			3S	Q	825					○A								×/-/-	×/-/-						
			3S	Q	826					×								×/-/-	×/-/-						
		C	3S	Q	874				○B	○								×/-/-	×/-/-						
		P	3S	/Q	876				○A	○															
		C	3S	Q	878				×	×															
		C	3S	/Q	879				×A	×															
			3S	Q	4374					○B															
			3S	Q	29825				×	×				○/-											
			3S	Q	29826				×	×				×/-											
	9	C	3S	Q	823					○A				○				×/-/-	×/-/-				○A		
		C	3S	/Q	824					×A								×/-/-	×/-/-						
		C	3S	Q	29823				×	×				×/-											
		C	3S	/Q	29824				×	×				×/-											
	10		3S	Q	821					○A					○A			×/-/-	×/-/-				○A		
			3S	/Q	822					×								×/-/-	×/-/-						
			3S	Q	1821					×															
			3S	Q	29821				○	×				○/-											
			3S	/Q	29822				×	×				×/-											
	10X2		3S	Q	16820																		H○		
			3S	Q	162820																		H○		
	16		3S	Q	16374										○A	H○	H○	○	○	○	○	○A/H○A	H○	○	
			3S	/Q	16534														×						
			3S	Q	162374											H○							H○		
	18	C	3S	Q	16823										○/○H			×	○				H○		
		C	3S	Q	162823										○A										
	20		3S	Q	16721												*						H○		
			3S	Q	16821										○		H○		×				H○		
			3S	Q	162721																		H○		
			3S	Q	162821																			×	
	22		3S	Q	16722																				○
	32		3S	Q	32374											H○	H○						H○A	H○	
			3S	Q	322374											H○									

Explanatory notes [Trigger] POS : Positive edge NEG : Negative Edge

[PRE・CLR] B : Preset and Clear C : Clear Only

[Output] 2S : Totem pole Output 3S : 3-State Output

[Q・/Q] B : Q・/Q-Output Q : Q-Output /Q : /Q-Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated

× : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

LATCH

Type	Curcuit	Output	PRE・CLR	Q・/Q	Device	Technology: Bipolar TTL	Bipolar LS	Bipolar S	Bipolar ALS	Bipolar AS	Bipolar F	CMOS HC	CMOS HCT	BiCMOS BCT	BiCMOS ABT	BiCMOS LVT	BiCMOS ALVT	Advanced CMOS AC	Advanced CMOS ACT	Advanced CMOS AHC	Advanced CMOS AHCT	Advanced CMOS LV	Advanced CMOS LVC	Advanced CMOS ALVC	Advanced CMOS AVC
S-R	4	2S		Q	279	×	○A																		
AD	8	2S		Q	259	×	○B		○			○/○	-/○					×/-/-	×/-/-						
	8	2S		Q	4724							×/-													
BIS	4	2S		Q	75	×	○					×/○	×/○					○/-/-							
	4	2S		Q	77							×/-													
	4	2S		Q	375		○					×/-													
	8	2S		Q	100	×																			
R/B	8	3S		Q	990				○																
	8	3S		/Q	991				×																
	8	3S	B	Q	666				○																
	8	3S	C	Q	996				○																
	8	3S	B	/Q	667				○																
	9	3S	C	Q	992				○																
	9	3S	C	/Q	993				×																
	10	3S		Q	994				○																
	10	3S		/Q	995				×																
D	8	2S	C	Q	116	×																			
	8	3S		Q	373		○	○	○A	○	○	○/○	○/○	○/-	○	H○		×/○/○	○/○/○	○	○	○A	○A	H○	
	8	3S		Q	2373						○														
	8	3S		/Q	533				○A	○A	×	×/○	×/○	×/-	○A			×/○/-	×/○/-						
	8	3S		Q	573				○C	○A	○	○A/○	○/○	○/-	○A	H○		×/○/○	×/○/○	○	○	○A	○A		
	8	3S		/Q	563				○B		×	○/○	×/○	×/-				×/○/○	×/○/-						
	8	3S		/Q	580				○B	×															
	8	3S	C	Q	873				○B	×A								×/-/-	×/-/-						
	8	3S	P	Q	880				×A	×															
	8	3S	B	Q	845				×	×								×/-/-	×/-/-						
	8	3S	B	Q	29845				×	×				×/-											
	8	3S	B	/Q	846				×	×								×/-/-	×/-/-						
	8	3S	B	/Q	29846				×	×				×/-											
	9	3S	B	Q	843					×					○			×/-/-	×/-/-						
	9	3S	B	Q	1843																				
	9	3S	B	Q	29843				×	×				○/-											
	9	3S	B	/Q	844				×	×								×/-/-	×/-/-						
	9	3S	B	/Q	29844				×	×				×/-											
	10	3S		Q	841				○	×A					○A			×/-/-	×/-/-				○A		
	10	3S		Q	29841				×	×				×/-											
	10	3S		/Q	842				×	×								×/-/-	×/-/-						
	10	3S		/Q	29842					×				×/-											
	12/24	3S		Q	16260										H○									H○	
	12/24	3S		Q	162260										H○									H○	
	16	3S		Q	16373										○A	H○	H○	○	○	○	○		○A/H○A	H○	○
	16	3S		/Q	16533													×							
	16	3S		Q	162373											H○								×	
	18	3S	B	Q	16843										○			×						×	
	20	3S		Q	16841										○			○						H○	
	20	3S		Q	162841										○									H○	
	32	3S		Q	32373											H○	H○						H○A		*

Explanatory notes [Type] S-R : S-R Latch AD : Addressable Latch BIS : Bistable Latch
R-B : Read-Back Latch D : D-Type Transparent Latch
[PRE・CLR] B : Preset and Clear C : Clear Only
[Output] 2S : Totem-Pole Output 3S : 3-State Output
[Q・/Q] B : Q・/Q-Output Q : Q-Output /Q : /Q-Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

SHIFT REGISTER

Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	Technology: Bipolar TTL	Bipolar LS	Bipolar S	Bipolar ALS	Bipolar AS	Bipolar F	CMOS HC	CMOS HCT	BiCMOS BCT	BiCMOS ABT	BiCMOS LVT	BiCMOS ALVT	Advanced CMOS AC	Advanced CMOS ACT	Advanced CMOS AHC	Advanced CMOS AHCT	Advanced CMOS LV	Advanced CMOS LVC	Advanced CMOS ALVC	Advanced CMOS AVC
S/P	S/P	4		R	2S	178	×																			
			C	R	2S	179	×																			
				R	2S	195	×	×	×		×		×/○													
				B	2S	95	×	×			×															
				B	2S	295		×C																		
			C	R	3S	395		×A																		
			C	B	2S	194	×	○A	×		○		×/○	-/○					×/-/-	×/-/-						
		5	C	R	2S	96	×	×																		
		8	C	R	3S	322		×					×/-													
			C	B	2S	198	×																			
			C	B	3S	299		○	×	○	×	○	×/○	-/○	×/-				×/-/○	×/-/○						
			C	B	3S	323		×		○	×	×			×/-				×/-/○	×/-/○						
			C	B	2S	199	×																			
S/P	S	8		R	2S	165	×	○A		○			○/○	-/○												
			C	R	2S	166	×	○A		○		×	○/○	-/○												
S	S/P	8	C	R	2S	164	×	○			○A		○/○	-/○					-/-/○	-/-/○						
S	P	10	C		2S	898													×/-/-	×/-/-						
S	S	8		R	2S	91	×	×																		
P	S	4	C	R	2S	94	×																			
		16		R	3S	674		○																		

SHIFT REGISTER WITH LATCH

Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	Technology: Bipolar TTL	Bipolar LS	Bipolar S	Bipolar ALS	Bipolar AS	Bipolar F	CMOS HC	CMOS HCT	BiCMOS BCT	BiCMOS ABT	BiCMOS LVT	BiCMOS ALVT	Advanced CMOS AC	Advanced CMOS ACT	Advanced CMOS AHC	Advanced CMOS AHCT	Advanced CMOS LV	Advanced CMOS LVC	Advanced CMOS ALVC	Advanced CMOS AVC
S/P	S/P	4	C	B	3S	671		×																		
		4	C	B	3S	672		×																		
		8	C	R	2S	598		○																		
S	S/P	8	C	R	3S	595		○					○/-								○	○	○A			
		8	C	R	OC	599		×																		
		8	C	R	OC	596		○																		
		8	C	R	2S	594		○					○/-								○	○	○A			
		16	C	B	3S	673		○																		
S/P	S	8	C	R	2S	597		○					-/○	-/○												

Explanatory notes [Input/Output Type] S : Serial P : Parallel S/P : Alternative Serial/Parallel
[CLR] C : With Clear
[Shift] R : Right-Shift B : Alternative Shift Right/Left
[Output] 2S : Totem-Pole Output 3S : 3-State Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

REGISTER(ETC)

Descriotion	Device	Technology																					
		Bipolar						CMOS		BiCMOS					Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
REGISTER FILES 8WX2B	172	×																			
REGISTER FILES 4WX4B	170	×	×																		
REGISTER FILES 4WX4B	670		○					-/○	-/○												
REGISTER FILES 16WX5B	870				○	×								×/-/-	×/-/-						
REGISTER FILES 16WX5B	858													×/-/-	×/-/-						
REGISTER FILES 16WX6B	871				×	×															
REGISTER FILES 32WX4B	859													×/-/-	×/-/-						
MUX WITH STRAGE	298	×	○			○A		×/-													
MUX WITH STRAGE	398		×																		
4BIT BUS-BUFFER REGISTER	173	×	○A					×/○	-/○												
8BIT STORAGE REGISTER	396		×																		
8BIT DIAGNOTICCS/PIPELINE REGISTER	818													×/-/-	×/-/-						
	819													×/-/-	×/-/-						
	29818				×					×/-											

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
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ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MONOSTABLE MULTIVIBRATOR

Curcuit	CLR	Retrigger	Device	Technology																			
				Bipolar						CMOS		BiCMOS					Advanced CMOS							
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
1			121	○																			
	C	R	122	×	○																		
	C	R	422		×																		
2	C	R	123	○	○					-/○	-/○							○A	○A	○A			
	C		221	○	○					-/○	-/○									○A			
	C	R	423		○					-/○	-/○												
	C	R	4538							-/○	-/○												

Explanatory notes [CLR] C : With Clear
[Retrigger] R : With Retrigger

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

DECADE/BINARY COUNTER

DEC・BIN	ASYN・SYN	No. of Bit	UP/DOWN Mode	CLR	LOAD	ETC	Device	Technology																					
								Bipolar						CMOS		BiCMOS				Advanced CMOS									
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
DEC	A	4		A			68		×																		
					9		90	×	○																		
							290	×	×																		
				A		D	390	×	○					×/○	-/○												
				A	A		176	×																			
				A	A		196	×	×	×																	
				A	9	D	490	×	×					×													
	S						560				×																
				S	S		162	×	×A	×	×B	×	×	×/-						×/-/-	×/-/-						
				A	S		160	×	×A		×B	×	×	×/-						×/-/-	×/-/-						
				A	S		690		×																		
				S	S		692		×																		
		4			S		568				×		×							×/-/-	×/-/-						
					S		168			×	×	×	×							×/-/-	×/-/-						
					S		668		×																		
			Y	A			190	×	×		×		×A	×/○						×/-/-	×/-/-						
				A	S		696		×																		
				S	S		698		×																		
				A	A		192	×	×		×			×/○						×/-/-	×/-/-						
		8		A		J	4017							×/○														
BIN	A	4		A			69		×																		
							93	×	○					-/○	-/○												
							293	×	○																		
				A		D	393	×	○					○/○	-/○									○A			
				A	A		177	×																			
				A	A		197	×	×	×																	
		7		A			4024							×/○	-/○												
		12		A			4040							○/○	-/○									○A			
		14		A			4020							○/○	-/○												
				A			4060							○/○	-/○												
				A			4061							×/-													
	S	4					561				○A																
				S	S		163	×	○A	○	○B	○	○A	○/○	-/○					×/-/○	×/-/○			○A			
				S	S		693		×																		
				A	S		161	×	○A		○B	○	○A	○/○	-/○					×/-/○	×/-/○			○A			
				A	S		691		×																		
						D	4518							-/○													
			Y		S		669		○																		
				S	S		699		×																		
					S		169		○B	×	○B	○A	○							×/-/-	×/-/-						
					A		191	×	○		○A			○/○	-/○					×/-/-	×/-/-						
				A	S		697		○																		
				A	A		193	×	○		○A		×A	○/○	-/○					×/-/-	×/-/-						
				A	A		569				○A		×							×/-/-	×/-/-						
		8		A	S		461													×/-/-	×/-/-						
				S	S		463													×/-/-	×/-/-						
				A	A	R	590		○					○A/-						×/-/-	×/-/-						
				A	A	R	591		×																		
				A	A	R	592		○											×/-/-	×/-/-						
				A	A	R	593		○											×/-/-	×/-/-						
				A		J	4022							×/-													
							4520							-/○													
				A		J	7022							×/-													
							40103							-/○													
			Y		S		469													×/-/-	×/-/-						
							579													×/-/-	×/-/-						
				S	S		869				○	○								×/-/-	×/-/-						
				A	S		867				○A	○								×/-/-	×/-/-						
OTH	A	1				12	92	×	○																		

Explanatory notes [DEC・BIN] DEC : Decoder BIN : Binary Counter OHE : Other
[ASYN・SYN] ASYN : Asynchronous SYN : Synchronous
[Up/Down] Y : Up/Down
[CLR] A : With Asynchronous Clear S : With Synchronous Clear
[LOAD] A : With Asynchronous Clear S : With Synchronous Clear 9 : Preset 9
[ETC] D : 2-Curcuit R : With Series Register J : Johnson Counter 12 : Devide By-Twelve Counter

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

RATE MULTIPLIER/FREQUENCY DIVIDERS

Descriotion	Device	Technology																			
		Bipolar						CMOS		BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
FREQUENCY DIVIDERS	56		×																		
FREQUENCY DIVIDERS	57		×																		
6BIT BINARY RATE MULTIPLIER	97	○																			
DECADE RATE MULTILIER	167	×																			
PROGRAMABLE FREQUENCY	292		○																		
DIVIDER/DIGITAL TIMERS	294		○																		

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

DATA SELECTOR/MULTIPLEXER

No. of Input/output	Output	Curcuit	ETC	Device	Technology																		
					Bipolar						CMOS		BiCMOS				Advanced CMOS						
					TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
16/1	2S	1		150	○												×/-/-	×/-/-						
	3S	1		250					○A								×/-/-	×/-/-						
	3S	1		850					×															
	3S	1		851					×															
	2S	1		4067							×/○													
8/1	2S	1		151	×A	○	○	○	○	○B	○/○	-/○					×/-/○	×/-/○						
	2S	1		152							×/-													
	3S	1		251	×	○	×	○	×	○B	○/○	-/○					×/-/○	×/-/×						
	3S	1		354		×					×/○	-/○												
	3S	1		356		×					×/-	-/○												
	3S	1		4051							-/○	-/○									○A			
	3S	1		4351							-/○	-/○												
	OC	1		355		×																		
	OC	1		357		×																		
4/1	2S	2		352		×		×	×	×	×/-						×/-/-	×/-/-						
	3S	2		153	×	○	×	○	○	○	○/○	-/○					×/-/○	×/-/○						
	3S	2		253		○		○	○A	○	○/○	-/○					×/-/○	×/-/○						
	3S	2		353		×		×	×	×	×/-						×/-/-	×/-/-						
	3S	2		4052							-/○	-/○									○A			
	3S	2		4352							-/○													
	3S	4		16460										H○									×	
	3S	4		162460										H○										
2/1	2S	1		157	×	○	○	○A	○	○A	○/○	○/○					×/-/○	×/-/○	○	○	○A	○A		
	2S	1		158		○	×	○	○	×A	○/○	-/○					×/-/○	×/-/○	○	○		-		
	2S	4	S	399		○																		
	3S	1		257		○B	○	○A	○	○	○/○	○/○					○-/○	○-/○				○A		
	3S	1		258		○B	×	○A	○	○	○/○	-/○					×/-/-	×/-/○				-		
	3S	4		4053							-/○	-/○									○A			
	3S	6	U	857				○	×															
	3S	8	S	604		×					×													
	OC	8	S	605		×																		
	3S	8	S	606		×																		
	OC	8	S	607		×																		
16	3S	16	AD	16254														×						

Explanatory notes [Output] 2S : Totem pole Output 3S : 3-State Output OC : Open-Collector Output
[ETC] S : Storage Register
Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

DECODER/DEMULTIPLEXER

No. of Input/output	Output	Curcuit	ETC	Device	Technology																		
					Bipolar						CMOS		BiCMOS				Advanced CMOS						
					TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
4/16	2S	1	AD	4514							×/○	-/○												
	2S	1	AD	4515							×/○	-/○												
	3S	1		154	○						×/○	-/○					×/-/-	×/-/-						
	OC	1		159	○																			
4/10	2S	1	BD	42	×A	○					○/○	-/○												
	2S	1	BD	43	×																			
	2S	1	BD	44	×																			
3/8	2S	1		238							×/○	-/○					×/-/○	×/-/○						
	2S	1		138		○	○A	○A	○	○	○/○	○/○					○/-/○	×/-/○	○	○	○A	○A		
	2S	1	AD	237							×/○	-/○												
	2S	1	AD	137		×		○A	×		×/○	×/○												
	2S	1	AD	131				×	×															
2/4	2S	2		139		○A	○A	○	×	×	○/○	○/○					×/-/○	○/-/○	○	○	○A	○A		
	2S	2		239							×/-						×/-/-	×/-/-						
	2S	2		155	×	○A																		
	OC	2		156	×	○			○															

Explanatory notes [Output] 2S : Totem pole Output 3S : 3-State Output OC : Open-Collector Output
[ETC] AD : Adress Latch BD : BCD TO DECIMAL
Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

CODE CONVERTER PRIORITY ENCODER/REGISTER

Descriotion	Device	Technology																			
		Bipolar						CMOS		BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
CODE CONVERTER	184	×																			
CODE CONVERTER	185	×																			
10-4 PRIORITY ENCODER	147	×	×					-/○	-/○												
8-3 PRIORITY ENCODER	148	×	○				×	○/-													
8-3 PRIORITY ENCODER	348		○									×									
4BIT CASCADABLE PRIORITY REGISTER	278	×																			

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

Display Decoder/Driver

Function	V_{OH} (V)	Device	Technology																					
			Bipolar						CMOS		BiCMOS					Advanced CMOS								
			TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
D	30	45	○																			
D	60	141	×																			
D	15	145	○	○																		
D	7	445		×																		
7	30	46	×																			
7	15	47	○A	○																		
7	5.5	48	×	×																		
7	5.5	49		×																		
7	30	246	×																			
7	15	247	×	○																		
7	7	347																				
7	7	447																				
7	5.5	248		×																		
7	5.5	249		×																		
B	7	142	×																			
B	7	143	×																			
B	7	144	×																			

Explanatory notes [Function] D : BCD TO DECIMAL、7 : BCD TO 7-SEGMENT、B : COUNTER/LATCH/DECODER/DRIVER
[V_{OH}] Off-Stage Output Voltage(V)

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

COMPARATOR

No. of Bit	Input	P=Q	$\overline{P=Q}$	P>Q	P<Q	Output	Device	Technology																	
								Bipolar						CMOS		BiCMOS				Advanced CMOS					
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
4	S	Y	N	V	V	2S	85	×	○	○		×		×A/○	-/○												
6	S	N	Y	N	N	2S	29806				×																
8	20	Y	N	N	N	OC	518				○		×														
8	20	N	Y	N	N	2S	520				○		×							×/-/-	×/-/-						
8	20	N	Y	N	N	OC	522				×																
8	20	N	Y	Y	N	2S	682		○					○/-													
8	20	N	Y	Y	N	OC	683		×																		
8	S	Y	N	N	N	OC	519				×		×														
8	S	N	Y	N	N	2S	521				○		○							×/-/-	×/-/-						
8	S	N	Y	Y	N	2S	684		○					○/-													
8	S	N	Y	Y	N	OC	685		×																		
8	S	N	Y	Y	N	2S	686		×																		
8	S	N	Y	Y	N	OC	687		×																		
8	S	N	Y	N	N	2S	688		○		○			○/○	-/○												
8	S	N	Y	N	N	OC	689		×		×																
8	S	Y	N	Y	Y	2S	860													×/-/-	×/-/-						
8	S	N	N	Y	Y	2S	865													×/-/-	×/-/-						
8	LP	N	N	Y	Y	2S	885					○								×/-/-	×/-/-						
8	LPQ	Y	N	Y	Y	OC	866					×A															
9	-	N	Y	N	N	2S	29809				×																

Explanatory notes [Input] S : Standard 20 : 20-kW Pullup Resistors LP : P-Port Latch LPQ : L,P-port Latch
[P=Q, P=$\overline{Q}$, P>Q, P<Q] Y : Yes N : No
[Output] 2S : Totem Pole Output. OC : Open-Collector Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ADRESS COMPARATOR、FUSE-PROGRAMMABLE IDENTITY COMPARATOR

Descriotion	No. of Bit	ETC	Device	Technology																				
				Bipolar						CMOS		BiCMOS				Advanced CMOS								
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
A	16-4	OE	677				×A			×						×/-/-	×/-/-						
A	16-4	L	678				×			×						×/-/-	×/-/-						
A	12-4	OE	679				○			×													
A	12-4	L	680				×			×													
F	16		526				×																
F	12		528				×																
F	8		527				×																

Explanatory notes [Function] A : Adress Comparator F : Fuse-Programmable Identity Comparators
[ETC] OE : Output-With Enable L : Output-With Latch

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

PARITY GENERATOR／CHECKER

No. of Bit	Device	Technology																						
		Bipolar						CMOS		BiCMOS				Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC			
8	180	×						×																
9	280		○	○	○	○	B	×/○	-/○					×/−/○	×/-/○									
9	286					○	×							×/-/-	○/-/-									

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

VOLTAGE CONTROLLED OSCILLATOR(VCO)

Curcuit	Fmax (MHz)	COMP'L Z OUT	ENABLE	RANGE INPUT	Rext	PLL	Device	Technology																	
								Bipolar						CMOS		BiCMOS				Advanced CMOS					
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
1	20	Y	Y	Y			624		○																		
	20	Y	Y	Y	Y		628		○																		
	24				Y	Y	7046							-/○	-/○												
2	20						627		×																		
	20		Y	Y			629		○																		
	20	Y					625		×																		
	20	Y	Y				626		×																		
	60		Y	Y			124			○																	
	24				Y	Y	4046							-/○													

Status ○ : Product available in technology indicated * : New product planned in technology indicated
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ACCUMULATORS, ARITHMETIC LOGIC UNIT(ALU), LOOK-AHEAD CARRY GENERATOR

Descriotion	Device	Technology																					
		Bipolar						CMOS		BiCMOS				Advanced CMOS									
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
4BIT PARALLEL BINARY ACCUMULATORS	281			×																	
4BIT PARALLEL BINARY ACCUMULATORS	681		×																		
4BIT ALU/FUNCTION GENERATORS	181	×	○	×		○A								×/-/-	×/-/-						
4BIT ALU/FUNCTION GENERATORS	381		×	×			×														
4BIT ALU/FUNCTION GENERATORS	881					×A								×/-/-	×/-/-						
4BIT ALU WITH RIPPLE CARRY	382		×				×														
LOOK AHEAD CARRY GENERATORS	264					×															
LOOK AHEAD CARRY GENERATORS	182	×		○		×															
LOOK AHEAD CARRY GENERATORS	282					×															
LOOK AHEAD CARRY GENERATORS	882					×A								×/-/-	×/-/-						
QUAD SERIAL ADDER/SUBTRACTOR	385		×																		

Status ○ : Product available in technology indicated * : New product planned in technology indicate
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ADDER

Descriotion	Device	Technology																					
		Bipolar						CMOS		BiCMOS				Advanced CMOS									
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
4BIT BINARY FULL ADDER	83	×	×																		
4BIT BINARY FULL ADDER	283	×	○	○			○	-/○	-/○					-/-/○	-/-/○						
DUAL CARRY SAVE FULL ADDER	183		×																		
GATED FULL ADDER	80	×																			
2BIT BINARY FULL ADDER	82	×																			

Status ○ : Product available in technology indicated * : New product planned in technology indicate
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MULTIPLIER

Descriotion	Device	Technology																					
		Bipolar						CMOS		BiCMOS				Advanced CMOS									
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
2-4 PARALLEL BINARY MULTIPLIERS	261		×																		
4-4 PARALLEL BINARY MULTIPLIERS	284	×																			
4-4 PARALLEL BINARY MULTIPLIERS	285	×																			
2'S COMPLEMENT MULTIPLIERS	384		×																		

Status ○ : Product available in technology indicated * : New product planned in technology indicate
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MEMORY

Descriotion	Device	Technology																					
		Bipolar						CMOS		BiCMOS				Advanced CMOS									
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
MEMORY REFRESH CONTROLLERS	600		×																		
MEMORY REFRESH CONTROLLERS	601		×																		
MEMORY REFRESH CONTROLLERS	603		×																		
MEMORY CYCLE CONTROLLER	608		×																		
MEMMORY MAPPERS	612		×																		
MEMMORY MAPPERS	613		×																		
MEMMORY MAPPERS WITH LATCH	610		×																		
MEMMORY MAPPERS WITH LATCH	611		×																		
MULTI-MODE LATCH	412			×																	
3-8 MEMORY DECIDER	2414									○/-											

Status ○ : Product available in technology indicated * : New product planned in technology indicate
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

CLOCK GENERATOR CIRCUIT

Descriotion	Device	Technology																					
		Bipolar						CMOS		BiCMOS				Advanced CMOS									
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
QUAD COMPLEMENTARY-OUTPUT LOGIC	265	×																			
DUAL PULSE SYNCHRONIZERS/DRIVERS	120	×																			
CRYSTAL-CONTOROLLED OSCILLATORS	320		×																		
CRYSTAL-CONTOROLLED OSCILLATORS	321		×																		
DIGITAL PHASE-LOCK LOOP	297		○					-/○	-/○						-/-/○						

Status ○ : Product available in technology indicated * : New product planned in technology indicate
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

SWITCH , SHIFTER , ERROR DETECTION CORRECTION CIRCUIT , HARD DISK DRIVER

Descriotion	Device	Technology																					
		Bipolar						CMOS		BiCMOS				Advanced CMOS									
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
QUAD BILATERAL SWITCHES	4016							-/○										○A			
	4066							○/○	-/○												
ANALOG SWITCHES WITH LEVEL TRANSLATION	4316							-/○	-/○												
4BIT SHIFTERS	350			×		×															
8BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	636		×																		
	637		×																		
16BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	616				×																
	617																				
	630		×																		
	631		×																		
32BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	632				×	×															
	633				×																
	634				×	×															
	635				×																
HARD DISK DRIVER	1250				×																

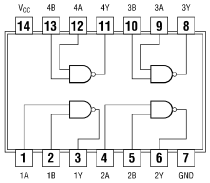
Status ○ : Product available in technology indicated * : New product planned in technology indicate
× : Discontinued ■ : Not recommended for new designs
HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

PIN ASSIGNMENTS

00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B}$

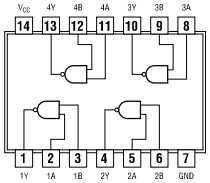


See page 139

01
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A \cdot B}$



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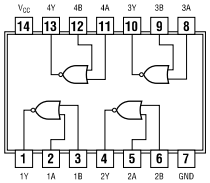
02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:

$Y = \overline{A + B}$



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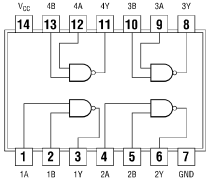
03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A \cdot B}$



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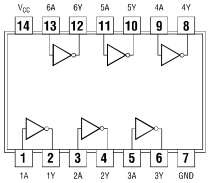
04
HEX INVERTERS

positive logic:

$Y = \overline{A}$



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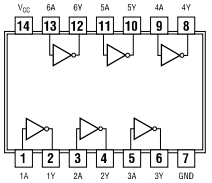
U04
HEX INVERTERS

positive logic:

$Y = \overline{A}$



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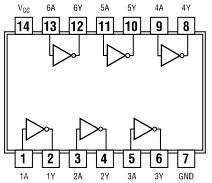
05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A}$

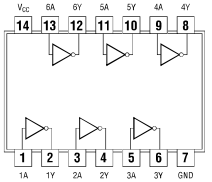


See page 144

06
HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = \overline{A}$

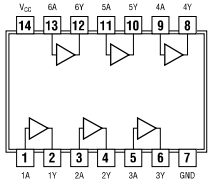


See page 145

07
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = \overline{A}$

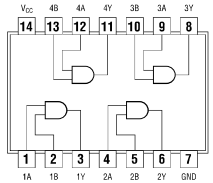


See page 145

08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \cdot B$

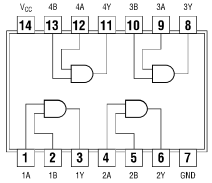


See page 146

09
QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = A \cdot B$

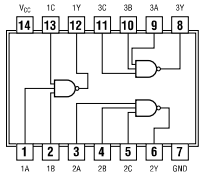


See page 147

10
TRIPLE 3-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B \cdot C}$

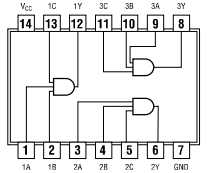


See page 148

11
TRIPLE 3-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \cdot B \cdot C$

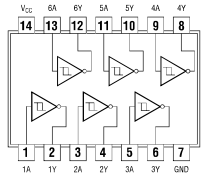


See page 149

14
HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$Y = \overline{A}$

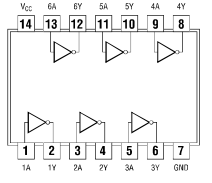


See page 150

16
HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = \overline{A}$

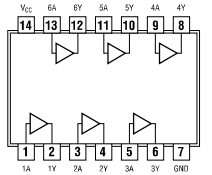


See page 151

17
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = A$

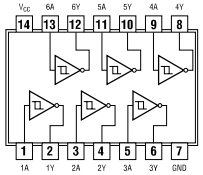


See page 151

19
HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$Y = \overline{A}$

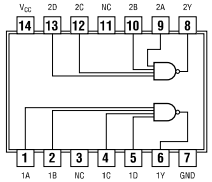


See page 152

20
DUAL 4-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B \cdot C \cdot D}$



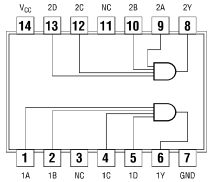
NC – No internal connection

See page 153

21
DUAL 4-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \cdot B \cdot C \cdot D$



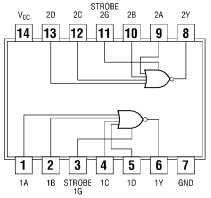
NC – No internal connection

See page 154

25
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:

$Y = G\,(\overline{A + B + C + D})$

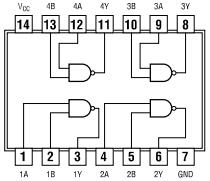


See page 154

26
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

positive logic:

$Y = \overline{AB}$

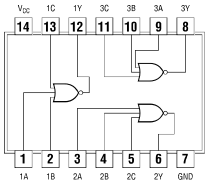


See page 155

27
TRIPLE 3-INPUT POSITIVE-NOR GATES

positive logic:

$Y = \overline{A + B + C}$

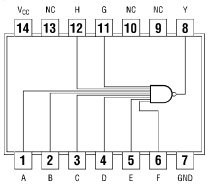


See page 155

30
8-INPUT POSITIVE-NAND GATES

positive logic:

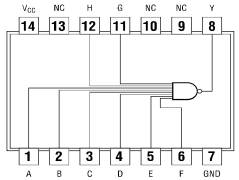
$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$



NC – No internal connection

See page 156

31
DELAY ELEMENTS



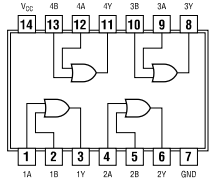
NC – No internal connection

See page 156

32
QUADRUPLE 2-INPUT POSITIVE OR GATES

positive logic:

$Y = A + B$

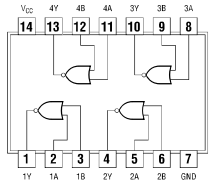


See page 157

33
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A + B}$

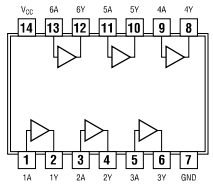


See page 158

35
HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = A$

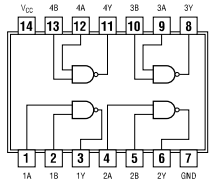


See page 158

37
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

positive logic:

$Y = \overline{A \cdot B}$

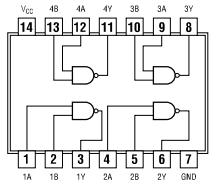


See page 159

38
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

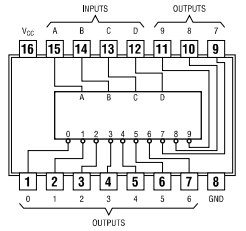
positive logic:

$Y = \overline{A \cdot B}$



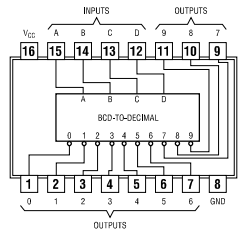
See page 159

42
4-LINE-TO-10-LINE DECODERS



See page 160

45
BCD-TO-DECIMAL DECODER/DRIVER



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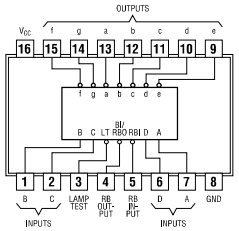
47
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS



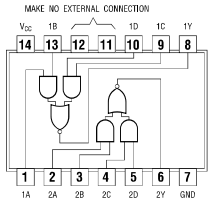
See page 164

51
AND-OR-INVERT GATES

'51, 'S51 DUAL 2-WIDE 2-INPUT

positive logic:

$Y = \overline{AB + CD}$



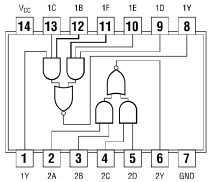
AND-OR-INVERT GATES

'LS51 2-WIDE 3-INPUT, 2-WIDE 2-INPUT

positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

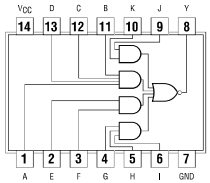


See page 166

64
4-2-3-2 INPUT AND-OR INVERT GATE

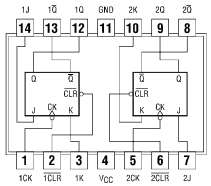
positive logic:

$Y = \overline{ABCD + EF + GHI + JK}$



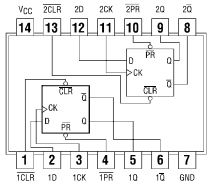
See page 167

73
DUAL J-K FLIP-FLOPS WITH CLEAR



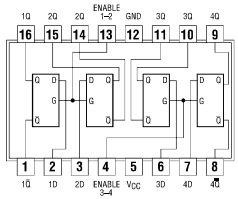
See page 168

74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



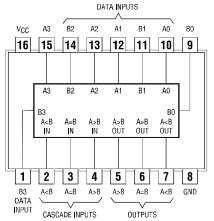
See page 170

75
4-BIT BISTABLE LATCHES



See page 172

85
4-BIT MAGNITUDE COMPARATORS



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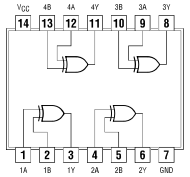
86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

positive logic:

$Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$



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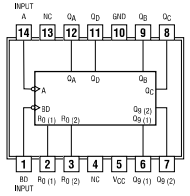
90
DECADE COUNTER



NC – No internal connection

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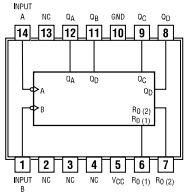
92
DIVIDE-BY-TWELVE COUNTERS



NC – No internal connection

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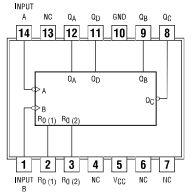
93
4-BIT BINARY COUNTERS



NC – No internal connection

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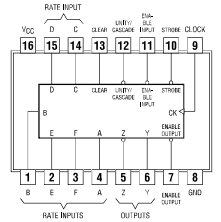
97
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIER



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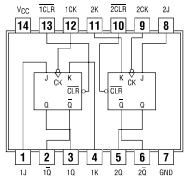
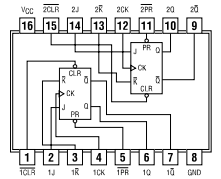
107
DUAL J-K FLIP-FLOPS WITH CLEAR



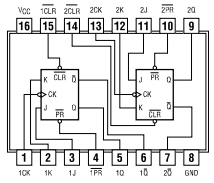
See page 180

109
DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



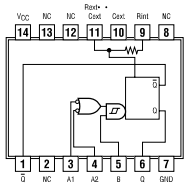
See page 182

112
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



See page 184

121
MONOSTABLE MULTIVIBRATOR



NC – No internal connection

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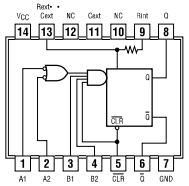
122
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR



NC – No internal connection

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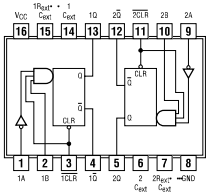
123
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBARATORS WITH CLEAR



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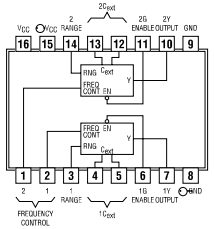
124
DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS



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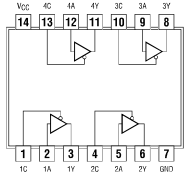
125
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

positive logic:

$Y = A$



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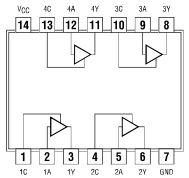
126
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

positive logic:

$Y = A$



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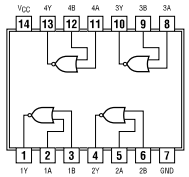
128
SN54128...75-Ω LINE DRIVER
SN74128...50-Ω LINE DRIVER

positive logic:

$Y = \overline{A + B}$



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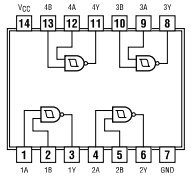
132
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

positive logic:

$Y = \overline{A \cdot B}$

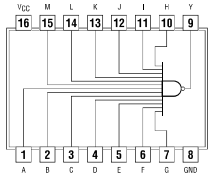


See page 192

133
13-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$

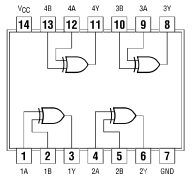


See page 193

136
QUAD 2-INPUT EXCLUSIVE-OR GATES WITH OPEN COLLECTOR OUTPUTS

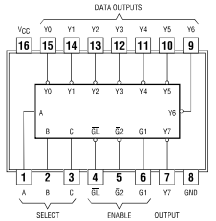
positive logic:

$Y = A \oplus B = \overline{A}B + A\overline{B}$



See page 193

137
3-TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES



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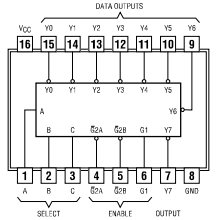
138
3-TO-LINE DECODERS/DEMULTIPLEXRS



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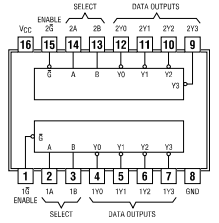
139
DUAL 2-TO-4-LINE DECODERS/DEMULTIPLEXERS



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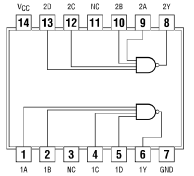
140
DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

positive logic:

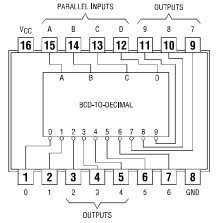
$Y = \overline{ABCD}$



NC – No internal connection

See page 200

145
BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS



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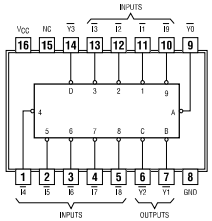
147
10-TO-4 LINE PRIORITY ENCODER



NC — No internal connection

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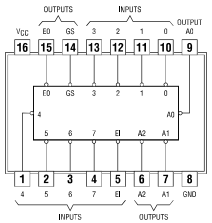
148
8-TO-3-LINE OCTAL PRIORITY ENCODERS



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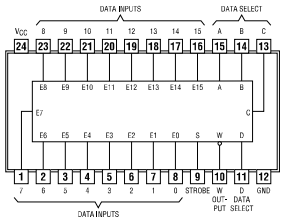
150
1-OF-16 DATA SELECTOR



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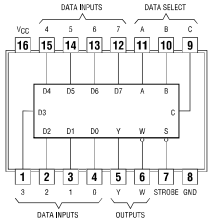
151
8-TO-1 LINE DATA SELECTORS/MULTIPLEXERS



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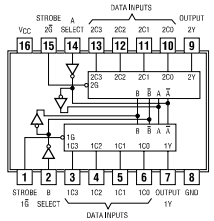
153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



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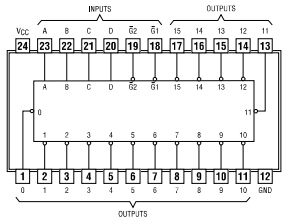
154
4-LINE TO 16-LINE DECODER/DEMULTIPLEXER



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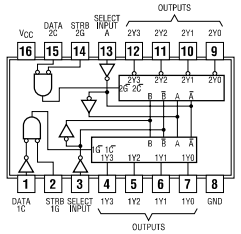
156
DECODERS/DEMULTIPLEXERS



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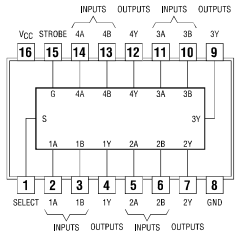
158
QUAD 2-TO 1-LINE DATA SELECTORS/MULTIPLEXERS



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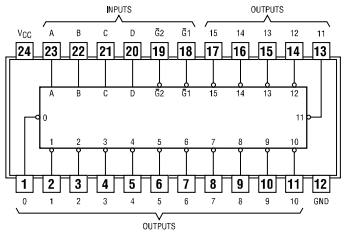
159
4-TO-16 LINE DECODER/DEMULTIPLEXER



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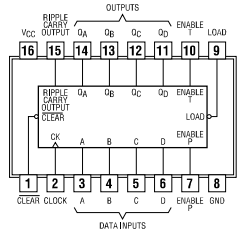
161
163
SYNCHRONOUS 4-BIT BINARY COUNTERS



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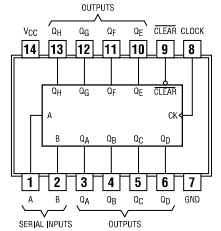
164
8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS



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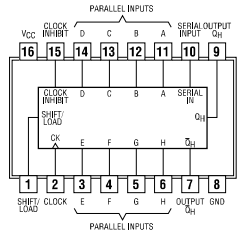
165
8-BIT SHFT REGISTERS



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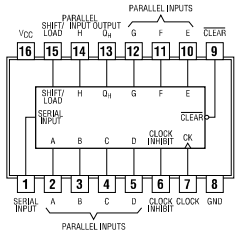
166
8-BIT SHIFT REGISTERS



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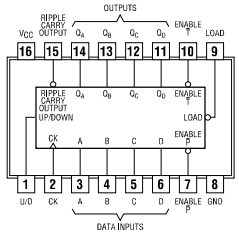
169
4-BIT UP/DOWN SYNCHRONOUS BINARY COUNTERS



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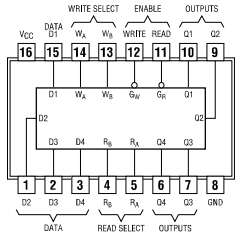
170
4-BY-4-REGISTER FILES



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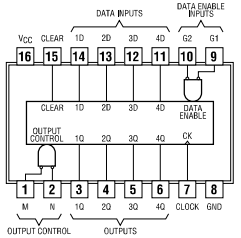
173
4-BIT D-TYPE REGISTERS



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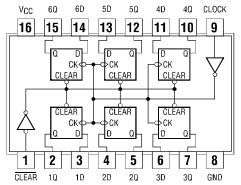
174
HEX D-TYPE FLIP-FLOPS



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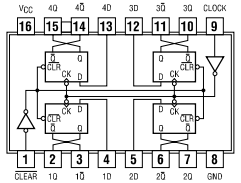
175
QUAD D-TYPE FLIP-FLOPS



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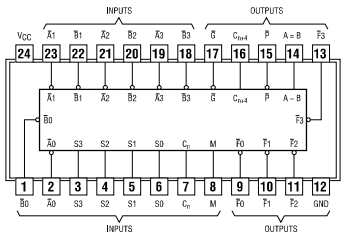
181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS



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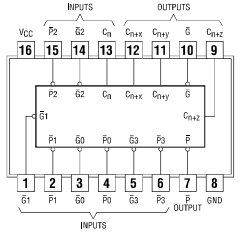
182
LOOK-AHEAD CARRY GENERATORS



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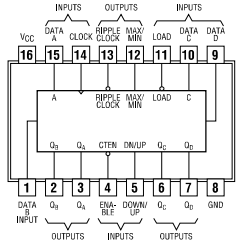
190
191
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS



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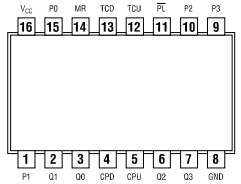
192
PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



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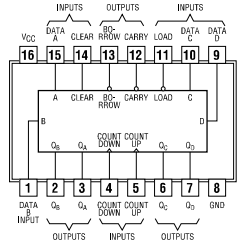
193
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS



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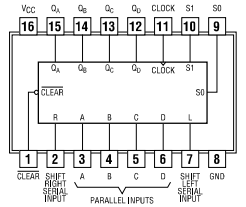
194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



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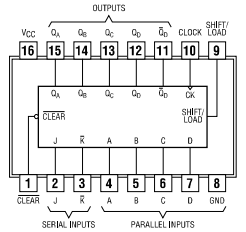
195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS



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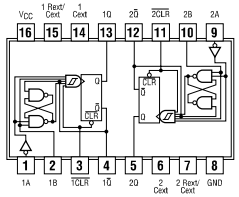
221
DUAL MONOSTABLE MULTIVIBRATORS



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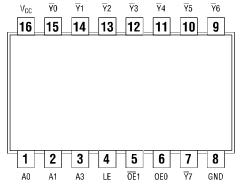
237
3-TO-8 LINE DECODER DEMULTIPLEXER WITH ADDRESS LATCHES



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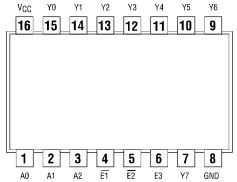
238
3-TO-8-LINE DECODERS/DEMULTIPLEXERS



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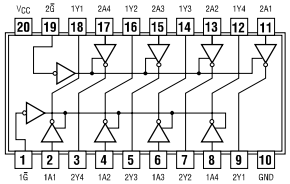
240
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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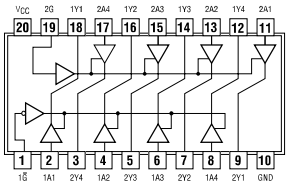
241
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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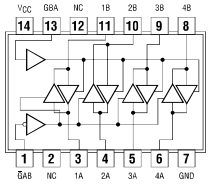
243
QUADRUPLE BUS TRANSCEIVERS



NC – No internal connection

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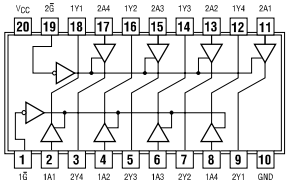
244
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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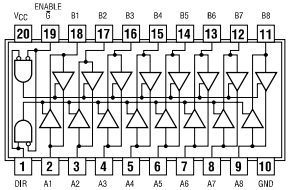
245
OCTAL BUS TRANSCEIVERS



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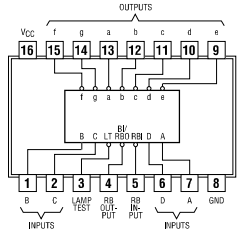
247 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS WITH RIPPLE BLANKING



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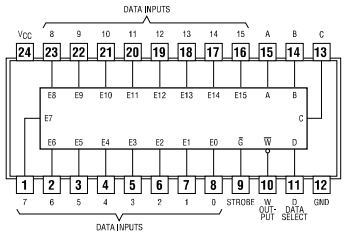
250
1-OF-16 DATA GENERATOR/MULTIPLEXER



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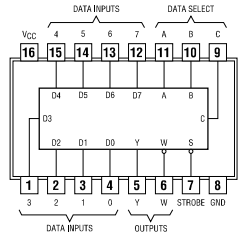
251
DATA SELECTORS/MULTIPLEXERS



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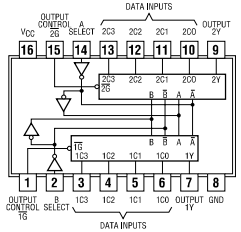
253
DUAL DATA SELECTORS/MULTIPLEXERS



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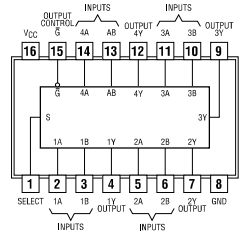
257
QUAD DATA SELECTORS/MULTIPLEXERS



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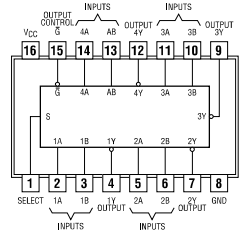
258
QUAD DATA SELECTORS/MULTIPLEXERS



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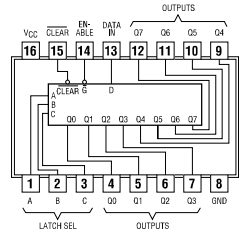
259
8-BIT ADDRESSABLE LATCHES



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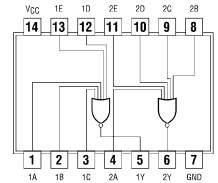
260
DUAL 5-INPUT POSITIVE-NOR GATES

positive logic:

$Y = A + B + C + D + E$



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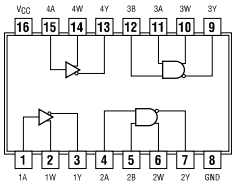
265
QUAD COMPLEMENTARY-OUTPUT ELEMENTS

positive logic:
Y = $\overline{A}$, W = A
Y = AB, W = AB



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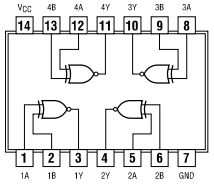
266
QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
Y = $\overline{A \oplus B}$



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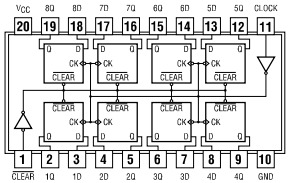
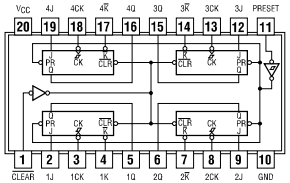
273
OCTAL D-TYPE FLIP-FLOPS



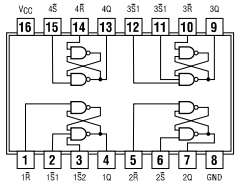
See page 291

276
QUAD J-$\overline{K}$ FLIP-FLORS



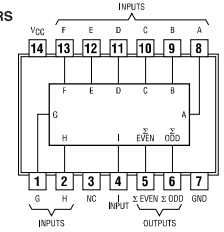
See page 292

279
QUAD $\overline{S}$-$\overline{R}$ LATCHES



See page 293

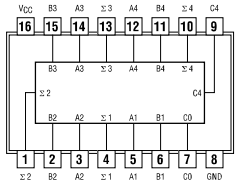
280
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS



NC – No internal connection

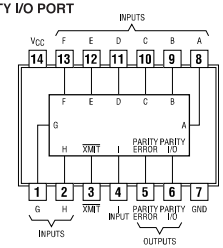
See page 294

283
4-BIT BINARY FULL ADDERS



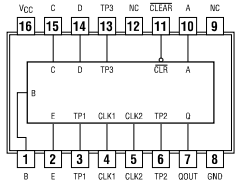
See page 296

286
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT



See page 298

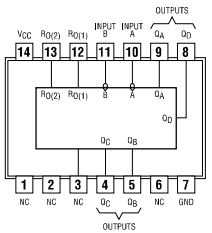
292
PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER



NC – No internal connection

See page 300

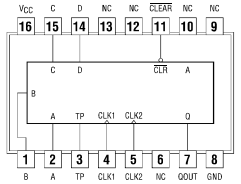
293
4-BIT BINARY COUNTERS



NC – No internal connection

See page 302

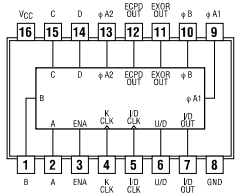
294
PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER



NC – No internal connection

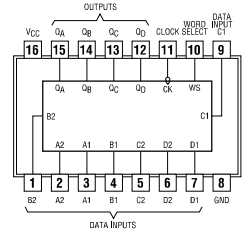
See page 304

297
DIGITAL PHASE-LOCKED-LOOP FILTERS



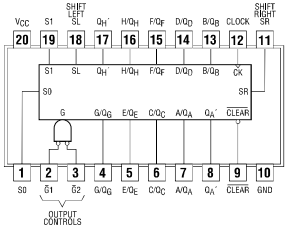
See page 306

298
QUAD 2-INPUT MULTIPLEXERS WITH STORAGE



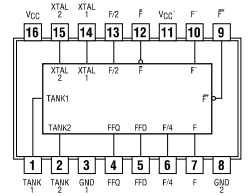
See page 308

299
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS



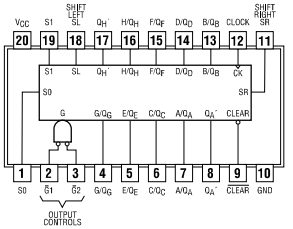
See page 310

321
CRYSTAL-CONTROLLED OSCILLATOR



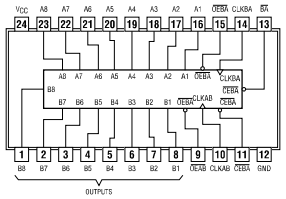
See page 312

323
8-BIT BIDIRECTIONAL SHIFT/STORAGE REGISTERS



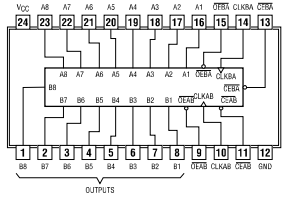
See page 314

2952
OCTAL BUS TRANSCEIVERS AND REGISTERS



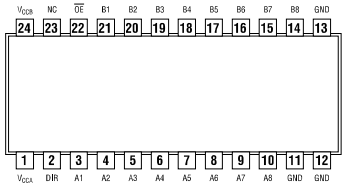
See page 492

2953
OCTAL BUS TRANSCEIVERS AND REGISTERS



See page 494

3245
OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS



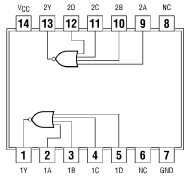
NC – No internal connection

See page 496

4002
DUAL 4-INPUT POSITIVE-NOR GATES

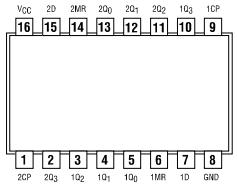
positive logic:

$Y = \overline{A + B + C + D}$



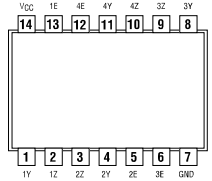
See page 497

4015
DUAL 4-STAGE STATIC SHIFT REGISTER



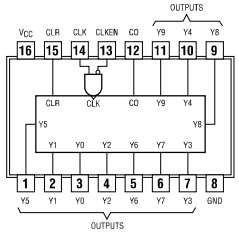
See page 498

4016
QUAD BILATERAL SWITCH



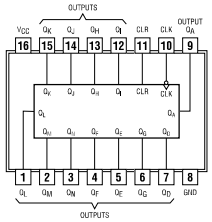
See page 499

4017
DECADE COUNTERS/DIVIDERS



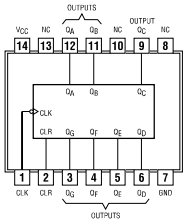
See page 500

4020
14-STAGE BINARY COUNTERS



See page 502

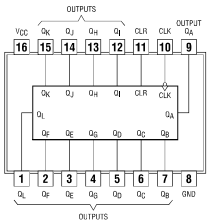
4024
7-STAGE BINARY COUNTERS



NC – No internal connection

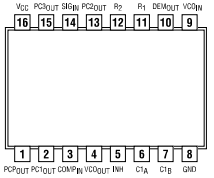
See page 503

4040
12-STAGE BINARY COUNTERS



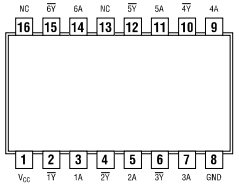
See page 504

4046
PHASE-LOCKED-LOOP WITH VCO



See page 505

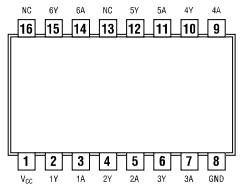
4049
HEX INVERTING BUFFERS



NC – No internal connection

See page 506

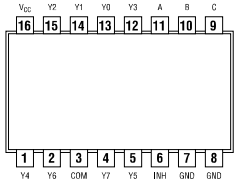
4050
HEX INVERTING BUFFERS NON-INVERTING



NC – No internal connection

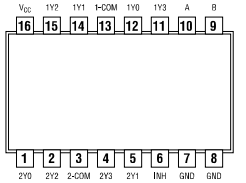
See page 506

4051
8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



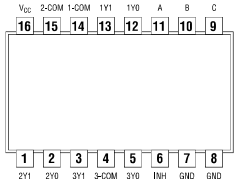
See page 507

4052
DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



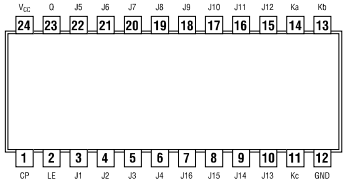
See page 508

4053
TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



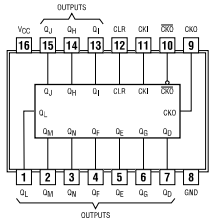
See page 509

4059
CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER



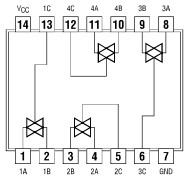
See page 510

4060
ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS



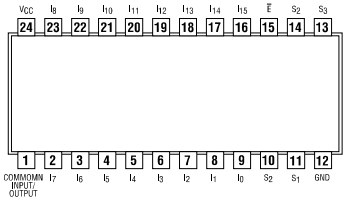
See page 511

4066
QUADRUPLE BILATERAL SWITCHES



See page 512

4067
16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

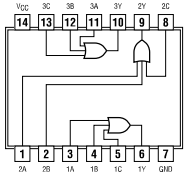


See page 513

4075
TRIPLE 3-INPUT OR GATES

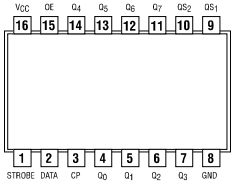
positive logic:

Y = A + B + C



See page 514

4094
8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE



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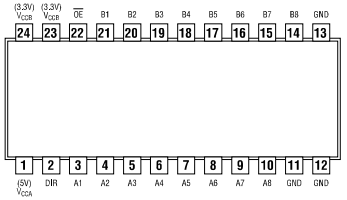
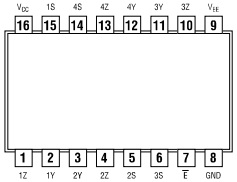
4245
OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS



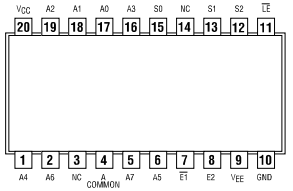
See page 518

4316
QUAD ANALOG SWITCH WITH LEVEL TRANSLATION



See page 519

4351
ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH



NC – No internal connection

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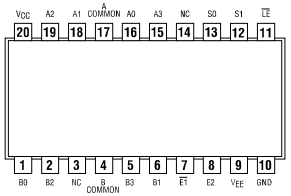
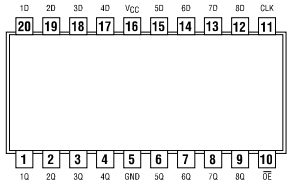
4352
ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH



NC – No internal connection

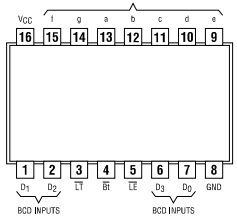
See page 521

4374
OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STAE OUTPUTS



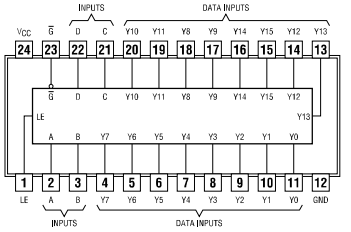
See page 522

4511
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS



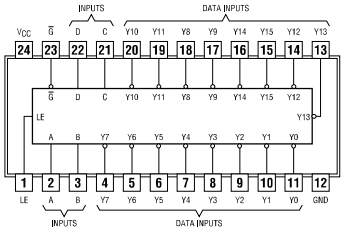
See page 523

4514
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH LATCHES



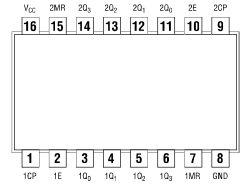
See page 524

4515
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH LATCHES



See page 526

4518
DUAL SYNCHRONOUS COUNTERS



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FUNCTION AND ELECTRICAL CHARACTERISTICS

00

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \bullet B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	22	4.4	36	3	17.4	10.2	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
I_{CC}	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
I_{OL}	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t_{PLH}	A or B	Y	MAX	22	15	4.5	11	4.5	6	23	27	25	30	7.4	8.5	7.3	12.3
t_{PHL}	A or B	Y	MAX	15	15	5	8	4	5.3	23	27	25	30	6.8	7	7.3	8.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t_{PLH}	A or B	Y	MAX	9.5	10.8	8.5	9	13	8.5	4.3	3
t_{PHL}	A or B	Y	MAX	8	13.2	8.5	9	13	8.5	4.3	3

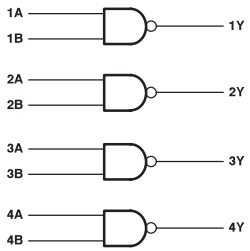
UNIT:ns

01

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

- $Y = \overline{A \bullet B}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	HC	UNIT
I_{CC}	MAX	22	4.4	3	0.02	mA
V_{OH}	MAX	5.5	5.5	5.5	V_{CC}	V
I_{OL}	MAX	16	8	8	4	mA

SWITCHING CHARACTERISTICS

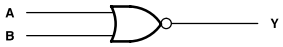
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	HC
t_{PLH}	A or B	Y	MAX	55	32	54	31
t_{PHL}	A or B	Y	MAX	15	28	28	25

UNIT:ns

02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

Logic Diagram



- $Y = \overline{A + B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	27	5.4	45	4	20.1	13	0.02	0.04	0.02	0.04	0.04	0.08	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.08	0.02	0.02	-	0.02	0.01	mA
I_{OH}	MAX	-24	-8	-8	-6	-12	-24	mA
I_{OL}	MAX	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11
t_{PLH}	A or B	Y	MAX	22	15	5.5	12	4.5	6.5	23	27	25	32	6.9	11.5	10.6
t_{PHL}	A or B	Y	MAX	15	15	5.5	10	4.5	5.3	23	27	25	32	6.4	11.5	8.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	A or B	Y	MAX	12.2	8.5	8.5	13	8.5	4.4
t_{PHL}	A or B	Y	MAX	12.2	8.5	8.5	13	8.5	4.4

UNIT: ns

03

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

Logic Diagram

- $Y = \overline{A \bullet B}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	22	4.4	36	4	0.02	0.04	0.04	mA
V_{OH}	MAX	5.5	8	5.5	8	0.05	Vcc	Vcc	V
I_{OL}	MAX	16	0.1	20	0.1	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A or B	Y	MAX	45	32	7.5	50	31	30	36
t_{PHL}	A or B	Y	MAX	15	28	7	13	25	30	36

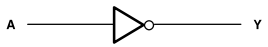
UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

04

HEX INVERTERS

Logic Diagram



- $Y = \overline{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	33	6.6	54	4.2	26.3	15.3	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
I_{CC}	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
I_{OL}	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t_{PLH}	A or B	Y	MAX	22	15	4.5	11	5	6	24	26	25	29	7.1	7.5	6.5	9.7
t_{PHL}	A or B	Y	MAX	15	15	5	8	4	5.3	24	26	25	29	6	7	6.5	9.6

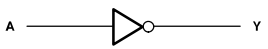
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t_{PLH}	A or B	Y	MAX	9	9.3	8.5	8.5	12	8.5	4.5	2.8
t_{PHL}	A or B	Y	MAX	8.5	9.3	8.5	8.5	12	8.5	4.5	2.8

UNIT: ns

U04

HEX INVERTERS

Logic Diagram



- $Y = \overline{A}$
- Unbuffered Output

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.02	0.04	0.02	-	0.02	0.01	mA
I_{OH}	MAX	-4	-4	-8	-6	-12	-24	mA
I_{OL}	MAX	4	4	8	6	12	24	mA

SWITCHING CHARACTERISTICS

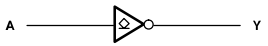
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V
t_{PLH}	A or B	Y	MAX	20	21	8	13	8	3.8
t_{PHL}	A or B	Y	MAX	20	21	8	13	8	3.8

UNIT: ns

05

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

Logic Diagram



- $Y = \overline{A}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V	UNIT
I_{CC}	MAX	33	6.6	54	4.2	0.02	0.08	0.08	0.02	-	0.02	mA
I_{OH}	MAX	-	-	-	-	-	-24	-24	-	-	-	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	5.5	5.5	5.5	Vcc	5.5	5.5	V
I_{OL}	MAX	16	8	20	8	4	24	24	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V
t_{PLH}	A or B	Y	MAX	55	32	7.5	54	29	-	-	-	12	8.5
t_{PHL}	A or B	Y	MAX	15	28	7	14	21	-	-	-	12	8.5
t_{PLZ}	A	Y	MAX	-	-	-	-	-	8.2	9.3	8.5	-	-
t_{PZL}	A	Y	MAX	-	-	-	-	-	6.5	10.8	8.5	-	-

UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

06

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

Logic Diagram

- $Y = \overline{A}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	51	60	-	0.02	0.01	mA
I_{OH}	MAX	0.25	0.25	-	0.0025	-	mA
V_{OH}	MAX	30	30	5.5	5.5	5.5	V
I_{OL}	MAX	40	40	8	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V
t_{PLH}	A or B	Y	MAX	15	15	12	8.5	3.7
t_{PHL}	A or B	Y	MAX	23	20	12	8.5	3.7

UNIT: ns

07

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

Logic Diagram

- $Y = A$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	41	45	-	0.02	0.01	mA
I_{OH}	MAX	0.25	0.25	-	0.0025	-	mA
V_{OH}	MAX	30	30	5.5	5.5	5.5	V
I_{OL}	MAX	40	40	8	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V
t_{PLH}	A or B	Y	MAX	15	10	12	8.5	2.9
t_{PHL}	A or B	Y	MAX	26	30	12	8.5	2.9

UNIT: ns

08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

Logic Diagram

- $Y = A \bullet B$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	33	8.8	57	4	24	12.9	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC	ALVC	UNIT
I_{CC}	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
I_{OL}	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t_{PLH}	A or B	Y	MAX	27	15	7	14	5.5	6.6	25	27	30	38	6.9	8.5	8.7	9
t_{PHL}	A or B	Y	MAX	19	20	7.5	10	5.5	6.3	25	27	30	38	6.5	7.5	8.7	8.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC	ALVC
t_{PLH}	A or B	Y	MAX	10	12.9	9	9	14	9	4.1	2.9
t_{PHL}	A or B	Y	MAX	10	12.9	9	9	14	9	4.1	2.9

UNIT: ns

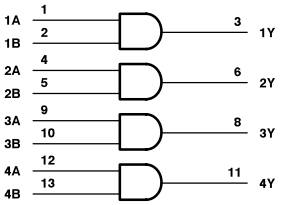
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

09

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

- Y = A•B

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	UNIT
I_{CC}	MAX	33	8.8	57	4.2	26.3	15.3	mA
I_{OH}	MAX	-	0.1	0.25	0.1	-	-	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	5.5	V_{CC}	mA
I_{OL}	MAX	16	8	20	8	20	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC
t_{PLH}	A or B	Y	MAX	32	35	10	54	9.6	31
t_{PHL}	A or B	Y	MAX	24	35	10	15	4.8	25

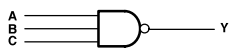
UNIT: ns

10

TRIPLE 3-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \bullet B \bullet C}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	16.5	3.3	27	2.2	13	7.7	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
I_{CC}	MAX	0.04	0.08	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-6	-12	-24	-24	mA
I_{OL}	MAX	24	24	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t_{PLH}	A, B or C	Y	MAX	22	15	4.5	11	4.5	6	24	30	19	36	6.7	8	12.2	8.9
t_{PHL}	A, B or C	Y	MAX	15	15	5	10	4.5	5.3	24	30	19	36	7	6.5	12.2	8.2

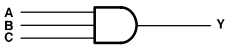
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVC
t_{PLH}	A, B or C	Y	MAX	10	-	13.5	9	4.9	3
t_{PHL}	A, B or C	Y	MAX	9.5	13.5	13.5	9	4.9	3

UNIT: ns

11

TRIPLE 3-INPUT POSITIVE-AND GATES

Logic Diagram



- Y = A•B•C
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	ACT 11	SN74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	6.6	42	3	18	9.7	0.02	0.04	0.02	0.04	0.04	0.02	0.04	0.02	-	0.02	mA
I_{OH}	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	-6	-12	mA
I_{OL}	MAX	8	20	8	20	20	4	4	4	4	24	24	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	ACT 11	SN74 ACT
t_{PLH}	A, B or C	Y	MAX	15	7	13	6	6.6	25	30	21	42	6.5	8.5	9.6	10.5
t_{PHL}	A, B or C	Y	MAX	20	7.5	10	5.5	6.5	25	30	21	42	6.9	7.5	8.7	10.5

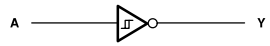
PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
t_{PLH}	A, B or C	Y	MAX	14	9
t_{PHL}	A, B or C	Y	MAX	14	9

UNIT: ns

14

HEX SCHMITT-TRIGGER INVERTERS

Logic Diagram



- Y = $\overline{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	UNIT
I_{CC}	MAX	60	21	0.02	0.04	0.02	0.04	0.02	0.08	0.02	0.08	0.02	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	-4	-24	-24	-24	-24	-8	-8	mA
I_{OL}	MAX	16	8	4	4	4	4	24	24	24	24	8	8	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
I_{CC}	MAX	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-6	-12	-24	-24	mA
I_{OL}	MAX	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT
t_{PLH}	A or B	Y	MAX	22	22	31	41	40	57	11	10.5	12.5	14.5
t_{PHL}	A or B	Y	MAX	22	22	31	41	40	57	9.5	10.5	11	9.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t_{PLH}	A or B	Y	MAX	12	9	18.5	12	6.4	3.4
t_{PHL}	A or B	Y	MAX	12	9	18.5	12	6.4	3.4

UNIT: ns

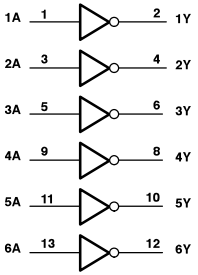
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

16

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

- $Y = \overline{A}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	51	mA
V_{OH}	MAX	15	V
I_{OL}	MAX	40	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A	Y	MAX	15
t_{PHL}	A	Y	MAX	23

UNIT: ns

17

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

- $Y = A$

Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	41	6.6
V_{OH}	MAX	15	V
I_{OL}	MAX	40	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A	Y	MAX	15
t_{PHL}	A	Y	MAX	26

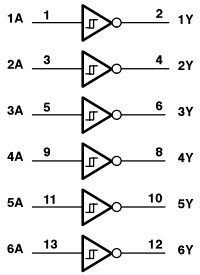
UNIT: ns

19

HEX SCHMITT-TRIGGER INVERTERS

- $Y = \overline{A}$
- P-N-P Input Reduce System Loading (I_{IL} = -0.05mA MAX)
- Excellent Noise Immunity with Typical Hysteresis of 0.8V

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	30	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_{PLH}	A or B	Y	MAX	20
t_{PHL}	A or B	Y	MAX	30

UNIT: ns

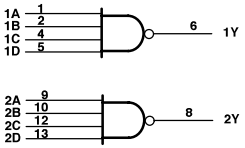
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

20

DUAL 4-INPUT POSITIVE-NAND GATES

- Y = $\overline{A \bullet B \bullet C \bullet D}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	11	2.2	18	1.5	8.7	5.1	0.02	0.04	0.04	0.04	0.08	0.04	0.08	-	0.02	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	24	24	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT
t_{PLH}	A, B, C or D	Y	MAX	22	15	4.5	11	5	6	28	30	42	6.7	12.2	9.1	13.5
t_{PHL}	A, B, C or D	Y	MAX	15	15	5	10	4.5	5.3	28	30	42	7.3	12.2	9.2	13.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
t_{PLH}	A, B, C or D	Y	MAX	11.5	8
t_{PHL}	A, B, C or D	Y	MAX	11.5	8

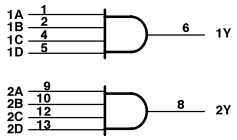
UNIT: ns

21

DUAL 4-INPUT POSITIVE-AND GATES

- Y = A•B•C•D
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
I_{CC}	MAX	4.4	2.3	12	7.3	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	8	8	20	20	4	4	4	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V
t_{PLH}	A, B, C or D	Y	MAX	15	15	6	5.3	28	33	41	8.8	9.8	12	6
t_{PHL}	A, B, C or D	Y	MAX	20	10	6	5.5	28	33	41	6.9	8.9	12	8

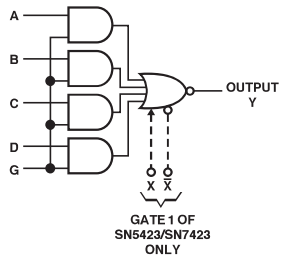
UNIT: ns

25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

- Y = $\overline{G\,(A + B + C + D)}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	19	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A or B	Y	MAX	22
t_{PHL}	A or B	Y	MAX	15

UNIT: ns

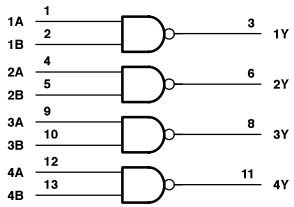
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

26

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

- $Y = \overline{AB}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	22	4.4	mA
V_{OH}	MAX	15	15	V
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_{PLH}	A or B	Y	MAX	24	32
t_{PHL}	A or B	Y	MAX	17	28

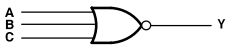
UNIT: ns

27

TRIPLE 3-INPUT POSITIVE-NOR GATES

- $Y = \overline{A + B + C}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
I_{CC}	MAX	26	6.8	4	17.1	12	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	8	20	20	4	4	4	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V
t_{PLH}	A, B or C	Y	MAX	15	15	15	5.5	5.5	23	29	35	7.7	10.1	14	9
t_{PHL}	A, B or C	Y	MAX	11	15	9	4.5	4.5	23	29	35	8.1	9.4	14	9

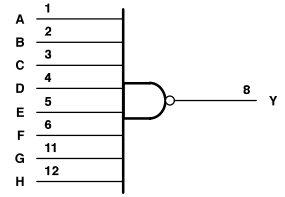
UNIT: ns

30

8-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	UNIT
I_{CC}	MAX	6	1.1	10	0.9	4.9	4	0.02	0.04	0.04	0.04	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11
t_{PLH}	A thru H	Y	MAX	22	15	6	10	5	5.5	33	39	42	7.2	8.5
t_{PHL}	A thru H	Y	MAX	15	20	7	12	4.5	5	33	39	42	7.4	8.7

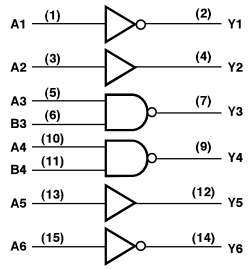
UNIT: ns

31

DELAY ELEMENTS

- Delay Elements for Generating Delay Line
- Inverting and Non-inverting Elements
- Buffer NAND Elements Rated at I_{OL} of 12/24mA
- P-N-P Inputs Reduce Fan-In (I_{IL} = -0.2mA MAX)
- Worst Case MIN/MAX Delays Guaranteed Across Temperature and V_{CC} Range

Logic Diagram



RECOMMENDED RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	20	mA
I_{OH}	Y3, Y4 outputs	MAX	-1.2	mA
	All other outputs	MAX	-0.4	mA
I_{OL}	Y3, Y4 outputs	MAX	24	mA
	All other outputs	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_{PLH}	A1, A6	Y1, Y6	MAX	65
t_{PHL}				45
t_{PLH}	A2, A5	Y2, Y5	MAX	80
t_{PHL}				95
t_{PLH}	A3, B3	Y3, Y4	MAX	15
t_{PHL}	A4, Y4			15

UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

32

QUADRUPLE 2-INPUT POSITIVE-OR GATES

● Y = A + B

Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	38	9.8	68	4.9	26.6	15.5	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
I_{CC}	MAX	0.02	0.08	0.02	0.02	0.02	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
I_{OL}	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC
t_{PLH}	A or B	Y	MAX	15	22	7	14	5.8	6.6	25	27	30	36	6.7	8.5
t_{PHL}	A or B	Y	MAX	22	22	7	12	5.8	-	25	27	30	36	5.9	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t_{PLH}	A or B	Y	MAX	9.5	9	10	12.1	8.5	9	13	8.5	3.8	2.8
t_{PHL}	A or B	Y	MAX	9.5	8	10	12.1	8.5	9	13	8.5	3.8	2.8

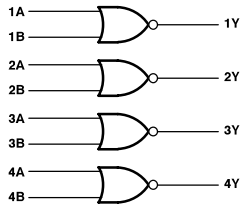
UNIT: ns

33

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

● $Y = \overline{A + B}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I_{CC}	MAX	16.5	13.8	9	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t_{PLH}	A or B	Y	MAX	15	32	33
t_{PHL}	A or B	Y	MAX	18	28	12

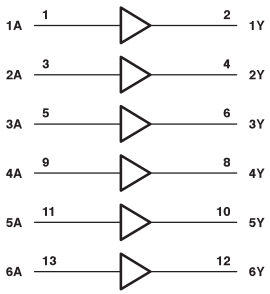
UNIT: ns

35

HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

● Y = A

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	63	mA
V_{OH}	MAX	5.5	V
I_{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	50
t_{PHL}	A	Y	MAX	14

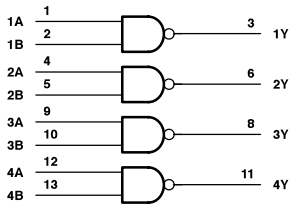
UNIT: ns

37

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

- $Y = \overline{A \cdot B}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
I_{CC}	MAX	54	12	80	7.8	33	mA
I_{OH}	MAX	-1.2	-1.2	-3	-2.6	-15	mA
I_{OL}	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
t_{PLH}	A or B	Y	MAX	22	24	6.5	8	6.5
t_{PHL}	A or B	Y	MAX	15	24	6.5	7	5

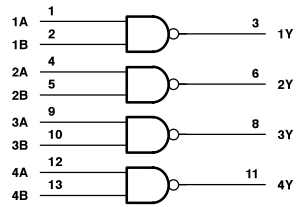
UNIT: ns

38

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- $Y = \overline{A \cdot B}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
I_{CC}	MAX	54	12	80	7.8	30	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	4.5	V
I_{OL}	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
t_{PLH}	A or B	Y	MAX	22	32	10	33	13
t_{PHL}	A or B	Y	MAX	18	28	10	12	5.5

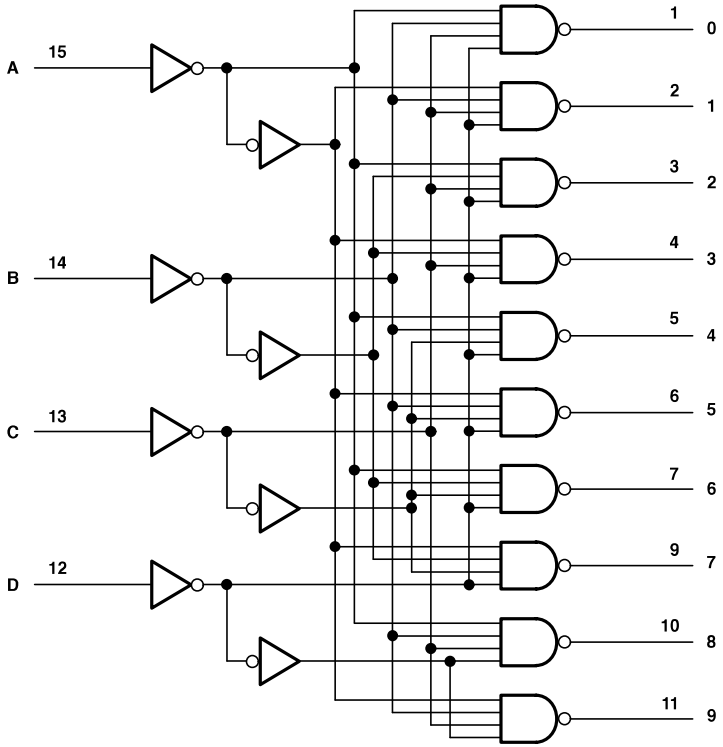
UNIT: ns

42

4-LINE TO 10-LINE DECODERS

- All Outputs Are High for Invalid Input Conditions
- Also for Applications as
  - 3-Line to 8-Line Decoders
  - 4-Line to 16-Line Decoders
- Full Decoding of Valid Input Logic Ensures That All Inputs Remain Off for All Invalid Input Conditions

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	56	13	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INTPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH} 2Level Logic	A, B, C or D	0-9	MAX	25	25	38	45	53
t_{PHL} 2Level Logic		0-9		25	25	38	45	53
t_{PLH} 3Level Logic	A, B, C or D	0-9	MAX	30	30	38	45	53
t_{PHL} 3Level Logic		0-9		30	30	38	45	53

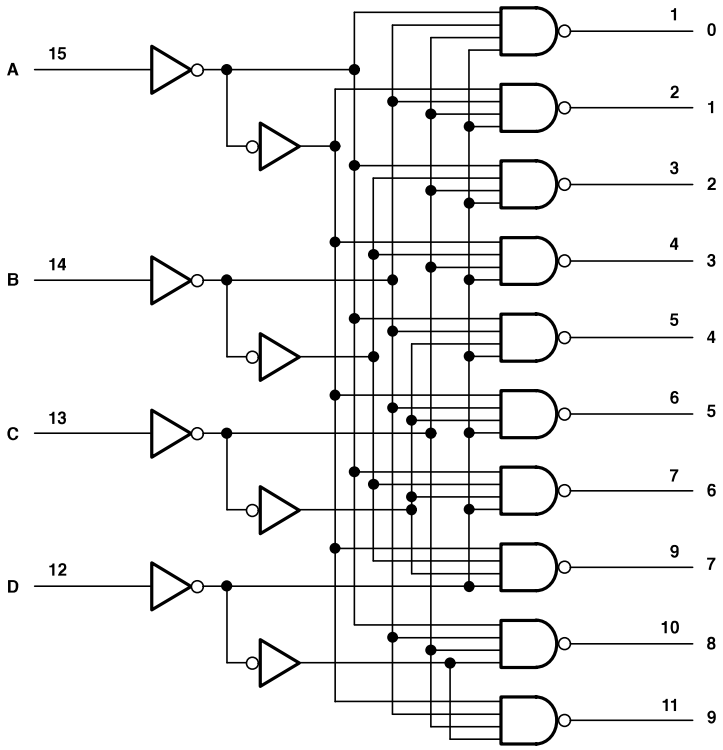
UNIT: ns

45

BCD-TO-DECIMAL DECODER/DRIVER

- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

Logic Diagram



FUNCTION TABLE

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	70	mA
$V_{O(on)}$	MAX	0.9	V
I_{OL}	MAX	80	mA

SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL
t_{PLH}	MAX	25
t_{PHL}		25

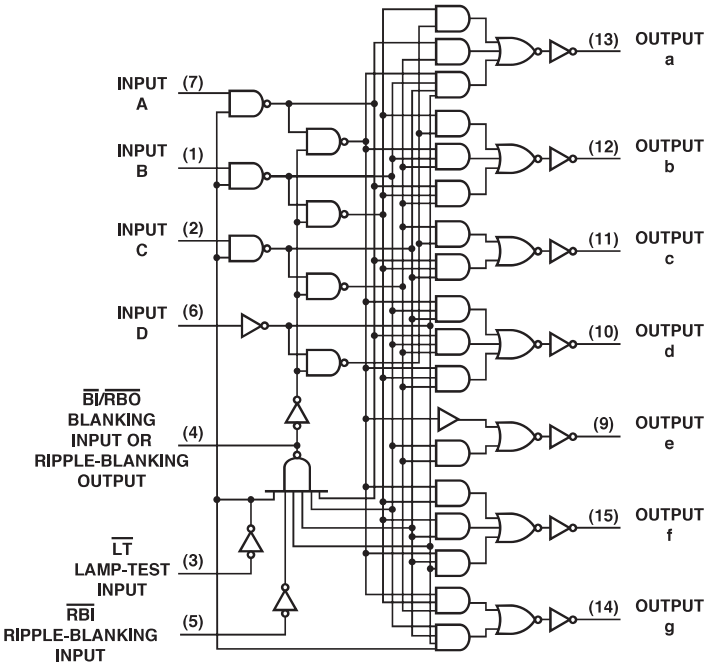
UNIT: ns

47

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

Logic Diagram



FUNCTION TABLE

No.	INPUTS					BI/RBO	OUTPUTS						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	103	13	mA
I_{OH}	MAX	-0.2	-0.05	mA
I_{OL}	MAX	8	3.2	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_{off}	A	A to g	MAX	100	100
t_{on}	A	A to g	MAX	100	100
t_{off}	RBI	A to g	MAX	100	100
t_{on}	RBI	A to g	MAX	100	100

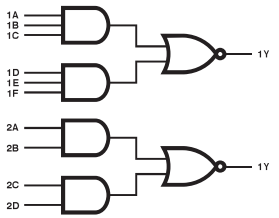
UNIT: ns

51

AND-OR INVERT GATES

- '51, 'S51: $Y = \overline{AB + CD}$
- 'F51, 'LS51: $1Y = \overline{(1A \bullet 1B \bullet 1C) + (1D \bullet 1E \bullet 1F)}$
- 'HC51: $2Y = \overline{(2A \bullet 2B) + (2C \bullet 2D)}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	F	SN74 HC	UNIT
I_{CC}	MAX	14	2.8	22	7.5	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-1	-1	-4	mA
I_{OL}	MAX	16	8	20	20	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	SN74 HC
t_{PLH}	Any	Y	MAX	22	20	5.5	6.5	35
t_{PHL}	Any	Y	MAX	15	20	5.5	4.5	35

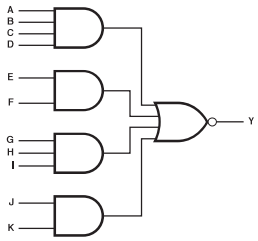
UNIT: ns

64

4-2-3-2 INPUT AND-OR INVERT GATE

● $Y = \overline{ABCD + EF + GHI + JK}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	F	UNIT
I_{CC}	MAX	16	4.7	mA
I_{OH}	MAX	-1	-1	mA
I_{OL}	MAX	20	20	mA

SWITCHING CHARACTERISTICS

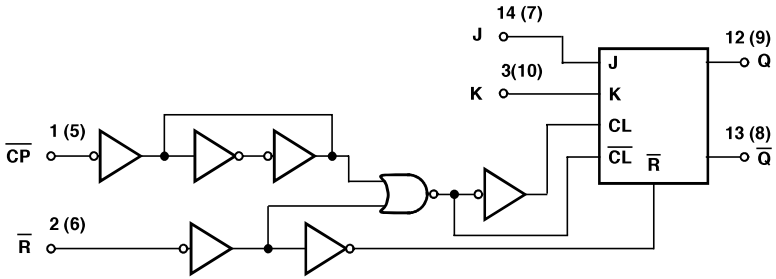
PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
t_{PLH}	Any	Y	MAX	5.5	7
t_{PHL}	Any	Y	MAX	5.5	5.5

UNIT: ns

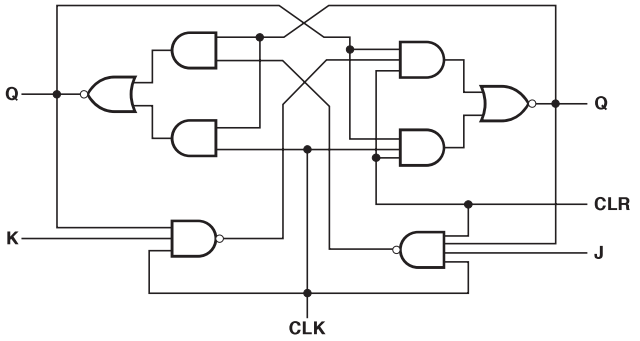
73

DUAL J-K FLIP-FLOPS WITH CLEAR

Logic Diagram



CD74HC/HCT73



'LS73

FUNCTION TABLE (SN74)

INPUTS				OUTPUTS	
$\overline{CLEAR}$	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

TRUTH TABLE (CD74)

INPUTS				OUTPUTS	
$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	No Change	
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	No Change	

NOTE:
H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↓ = High-to-Low Transition

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	20	6	0.04	0.08	0.08	mA
I_{OH}	MAX	16	8	4	4	4	mA
I_{OL}	MAX	-0.4	-0.4	-4	-4	-4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	15	30	25	20	20
tw	CLOCK"L"			MIN	20	-	20	-	-
	CLOCK"H"				47	20	20	-	-
	$\overline{CP}$ Pulse Wide				-	-	-	24	24
	$\overline{CLEAR}$ "L"				25	20	20	24	27
tsu	CLK			MIN	0	20	25	-	-
	J,K to $\overline{CP}$				-	-	-	24	24
th	CLK			MIN	0	0	0	-	-
	J,K to $\overline{CP}$				-	-	-	3	3
t_{PLH}		$\overline{CLEAR}$	$\overline{Q}$	MAX	25	20	39	44	51
t_{PHL}					-	20	39	44	51
t_{PLH}		$\overline{CLEAR}$	Q	MAX	-	20	39	44	51
t_{PHL}					40	20	39	44	51
t_{PLH}		CLOCK	Q or $\overline{Q}$	MAX	25	20	32	-	-
t_{PHL}					40	20	32	-	-
t_{PLH}		$\overline{CP}$	Q	MAX	-	-	-	48	57
t_{PHL}					-	-	-	48	57
t_{PLH}		$\overline{CP}$	$\overline{Q}$	MAX	-	-	-	48	54
t_{PHL}					-	-	-	48	54

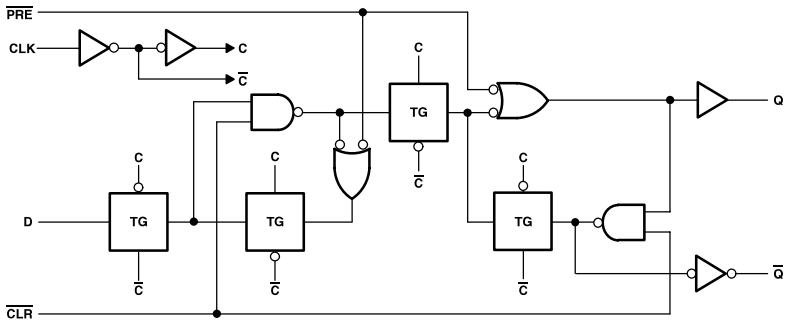
UNIT fmax : MHz, other : ns

74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{\text{PRESET}}$	$\overline{\text{CLEAR}}$	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↓	H	H	L
H	H	↓	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

† This configuration is unstable, that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	15	8	25	4	16	16	0.04	0.08	0.04	0.08	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	mA
I_{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	mA
I_{OL}	MAX	24	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11
fmax				MIN	15	25	75	34	105	100	25	20	24	16	125
tw	CLOCK"H"			MIN	30	25	6	14.5	4	4	20	24	23	27	4
	CLOCK"L"			MIN	37	-	7.3	14.5	5.5	5	20	24	23	27	4
	$\overline{\text{RESET}}$ or $\overline{\text{CLEAR}}$ "L"			MIN	30	25	7	15	4	4	25	24	20	24	4
tsu	D			MIN	20	20	3	15	4.5	3	25	18	15	18	3.5
	$\overline{\text{PRE}}$, $\overline{\text{CLR}}$ INACTIVE			MIN	20	-	-	10	2	2	6	-	0	5	1
th				MIN	5	5	2	0	0	1	0	3	0	3	0
t_{PLH}		$\overline{\text{RESET}}$	Q	MAX	25	25	6	13	7.5	7.1	58	60	44	60	7.1
t_{PHL}			$\overline{Q}$		40	40	13.5	15	10.5	10.5	58	60	44	60	9
t_{PLH}		$\overline{\text{CLEAR}}$	$\overline{Q}$	MAX	25	25	6	13	7.5	7.1	58	60	44	60	7.1
t_{PHL}			Q		40	40	13.5	15	10.5	10.5	58	60	44	60	9
t_{PLH}		CLOCK	Q or $\overline{Q}$	MAX	25	25	9	16	8	7.8	44	53	35	53	8.2
t_{PHL}					40	40	9	18	9	9.2	44	53	35	53	7.5

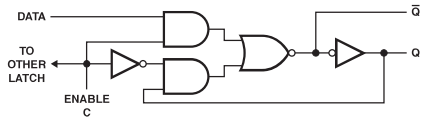
PARAMETER		INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
fmax				MIN	125	110	85	125	85	75	65	45	75	100
tw	CLOCK"H"			MIN	5	4.5	5	6	5.7	5	5	7	5	3.3
	CLOCK"L"			MIN	5	4.5	5	6	5.7	5	5	7	5	3.3
	$\overline{\text{RESET}}$ or $\overline{\text{CLEAR}}$ "L"			MIN	5	4	5	6	5	5	5	7	5	3.3
tsu	D			MIN	3	3.5	4.5	3.5	4	5	5	7	5	3
	$\overline{\text{PRE}}$, $\overline{\text{CLR}}$ INACTIVE			MIN	0	-	2	0	-	3	3.5	5	3	2
th				MIN	0.5	0	0	1	9.5	0.5	0	0.5	0.5	0
t_{PLH}		$\overline{\text{RESET}}$	Q	MAX	10	10.5	9.6	11.5	11.5	11	13	18	11	5.4
t_{PHL}			$\overline{Q}$		10.5	11.5	12.5	12.5	12.5	11	13	18	11	5.4
t_{PLH}		$\overline{\text{CLEAR}}$	$\overline{Q}$	MAX	10	10.5	9.6	11.5	11.5	11	13	18	11	5.4
t_{PHL}			Q		10.5	11.5	12.5	12.5	12.5	11	13	18	11	5.4
t_{PLH}		CLOCK	Q or $\overline{Q}$	MAX	10.5	10	9.4	14	9.5	10.5	10	17.5	10.5	5.2
t_{PHL}					10.5	10	8.8	12	9.5	10.5	10	17.5	10.5	5.2

UNIT fmax : MHz, other : ns

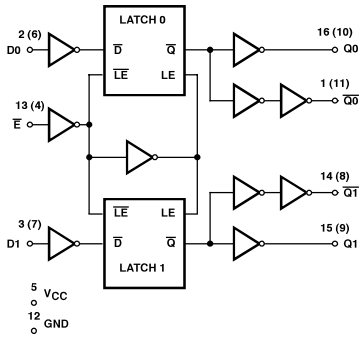
75

4-BIT BISTABLE LATCHES

Logic Diagram



SN74LS75



CD74HC/HCT75

FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q_0}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	53	12	0.04	0.08	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
tw			MIN	20	20	20	24	24
tsu				20	20	25	18	18
th			MIN	5	5	5	3	3
t_{PLH}	D	Q	MAX	30	27	30	33	42
t_{PHL}				25	17	30	33	42
t_{PLH}	D	$\overline{Q}$	MAX	40	20	30	39	42
t_{PHL}				15	15	30	39	42
t_{PLH}	G	Q	MAX	30	27	33	39	42
t_{PHL}				15	25	33	39	42
t_{PLH}	G	$\overline{Q}$	MAX	30	30	33	39	45
t_{PHL}				15	15	33	39	45

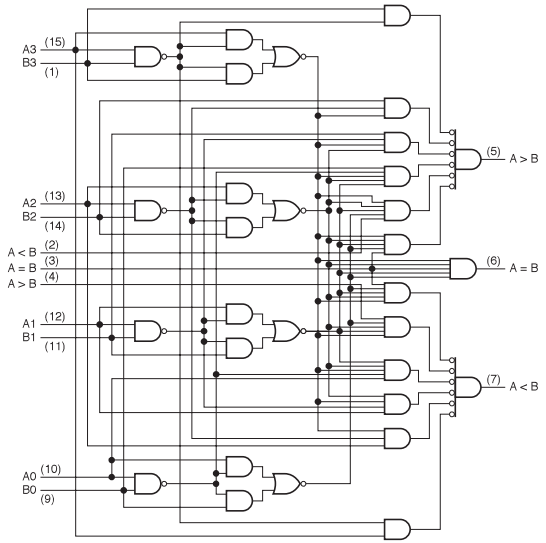
UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

85

4-BIT MAGNITUDE COMPARATORS

Logic Diagram



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	88	20	115	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.4	-0.4	-1	-4	-4	-4	mA
I_{OL}	MAX	16	8	20	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	Nunber of Gate Levels	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	Any A or B data input	A B, A B	3	MAX	26	36	16	58	59	56
		A B	4	MAX	35	45	18	50	53	60
t_{PHL}	Any A or B data input	A B, A B	3	MAX	30	30	16.5	58	59	56
		A B	4	MAX	30	45	16.5	50	53	60
t_{PLH}	A B, A B	A B	1	MAX	11	22	7.5	44	42	45
t_{PHL}	A B, A B	A B	1		17	17	8.5	44	42	45
t_{PLH}	A B	A B	2	MAX	20	20	10.5	37	-	-
t_{PHL}	A B	A B	2		17	26	7.5	37	-	-
t_{PLH}	A B, A B	A B	1	MAX	11	22	7.5	44	42	47
t_{PHL}	A B, A B	A B	1		17	17	8.5	44	42	47

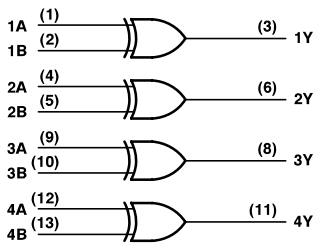
UNIT: ns

86

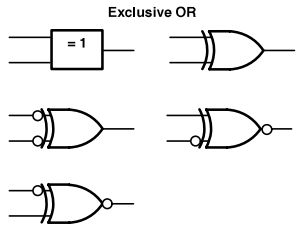
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

- $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$
- 74AC11xxx : Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	50	10	75	5.9	38	28	0.02	0.04	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	16	8	20	8	20	20	4	4	4	24	24	24	24	mA
I_{OL}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.04	0.08	0.02	0.02	-	0.02	0.01	mA
I_{OH}	MAX	24	24	8	8	6	12	24	mA
I_{OL}	MAX	-24	-24	-8	-8	-6	-12	-24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t_{PLH}	A or B	Y	MAX	23	23	10.5	17	7.5	6.5	25	36	48	7.6	9	10.8	9.6
t_{PHL}		Y	MAX	17	17	10	12	6.5	6.5	25	36	48	6.8	9.5	10.8	9
t_{PLH}	A or B	Y	MAX	30	30	10.5	17	6.5	8	25	36	48	7.6	9	10.8	9.6
t_{PHL}		Y	MAX	22	22	10	10	7	7.5	25	36	48	6.8	9.5	10.8	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH} Input Low	A or B	Y	MAX	10	14.6	10	10	16.5	10	4.6
t_{PHL} Input Low		Y	MAX	10.5	14.6	10	10	16.5	10	4.6
t_{PLH} Input High	A or B	Y	MAX	10	14.6	10	10	16.5	10	4.6
t_{PHL} Input High		Y	MAX	10.5	14.6	10	10	16.5	10	4.6

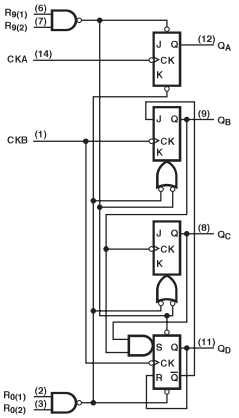
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

90

DECADE COUNTER

Logic Diagram



FUNCTION TABLE

BCD COUNT SEQUENCE

Count	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY

Count	OUTPUTS			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUTS			
$R0_{(1)}$	$R0_{(2)}$	$R9_{(1)}$	$R9_{(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	39	15	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

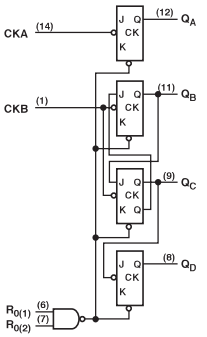
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax		A	QA	MIN	32	32
		B	QB		16	16
tw	A			MIN	15	15
	B				30	30
	RESET				15	30
tsu	RESET INACTIVE			MIN	25	25
t_{PLH}		A	QA	MAX	16	16
t_{PHL}					18	18
t_{PLH}		A	QD	MAX	48	48
t_{PHL}					50	50
t_{PLH}		B	QB	MAX	16	16
t_{PHL}					21	21
t_{PLH}		B	QC	MAX	32	32
t_{PHL}					35	35
t_{PLH}		B	QC	MAX	32	32
t_{PHL}					35	35
t_{PHL}		Set to 0	Any	MAX	40	40
t_{PLH}		Set to 9	QA, QD	MAX	30	30
t_{PHL}			QB, QC		40	40

UNIT fmax : MHz, other : ns

92

DIVIDE-BY-12 COUNTERS

Logic Diagram



FUNCTION TABLE

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

RESET INPUTS		OUTPUTS			
$R0_{(1)}$	$R0_{(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	39	15	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax		A	QA	MIN	32	32
		B	QB		16	16
tw	A			MIN	15	15
	B				30	30
	RESET				15	30
tsu	RESET INACTIVE			MIN	25	25
t_{PLH}		A	QA	MAX	16	16
t_{PHL}					18	18
t_{PLH}		A	QD	MAX	48	48
t_{PHL}					50	50
t_{PLH}		B	QB	MAX	16	16
t_{PHL}					21	21
t_{PLH}		B	QC	MAX	16	16
t_{PHL}					21	21
t_{PLH}		B	QD	MAX	32	32
t_{PHL}					35	35
t_{PHL}		Set to 0	Any	MAX	40	40

UNIT fmax : MHz, other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

93

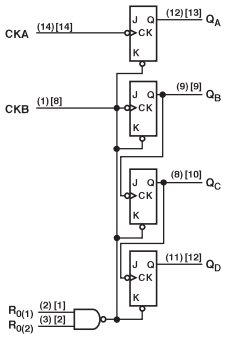
4-BIT BINARY COUNTERS

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

RESET INPUTS		OUTPUTS			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	39	15	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT
fmax		A	QA	MIN	32	32	20	20
		B	QB		16	16	20	20
tw	A			MIN	15	15	24	24
	B				30	30	24	24
	RESET				15	30	24	24
tsu	RESET INACTIVE			MIN	25	25	-	-
							-	-
t_{PLH}		A	QA	MAX	16	16	38	51
t_{PHL}					18	18	38	51
t_{PLH}		A	QD	MAX	70	70	-	87
t_{PHL}					70	70	-	87
t_{PLH}		B	QB	MAX	16	16	41	51
t_{PHL}					21	21	41	51
t_{PLH}		B	QC	MAX	32	32	56	69
t_{PHL}					35	35	56	69
t_{PLH}		B	QD	MAX	51	51	74	87
t_{PHL}					51	51	74	87
t_{PHL}		Set to 0	ANY	MAX	40	40	-	-

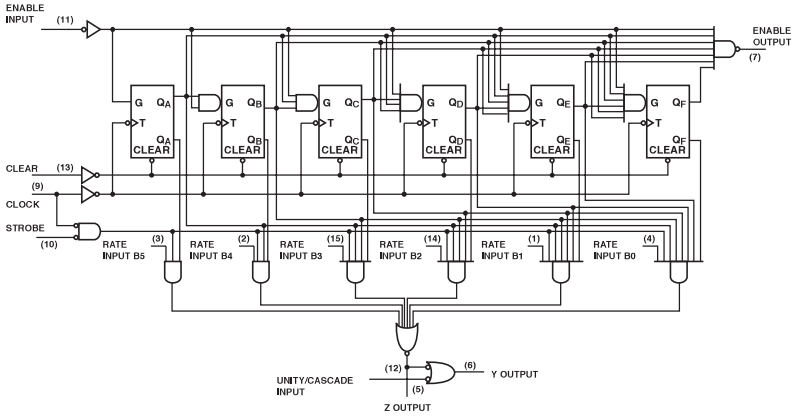
UNIT fmax : MHz, other : ns

97

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIER

- Perform Fixed-Rate or Variable-Rate Frequency Division
- Typical Maximum Clock Frequency: 32MHz

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS								OUTPUTS		
			BINARY RATE					LOGI LEVEL OR NUMBER OF PULSES		
CLEAR	ENABLE	STROBE	F	E	D	C	B	A	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE
H	X	H	X	X	X	X	X	X	X	H	L	H	H
L	L	L	L	L	L	L	L	L	64	H	L	H	1
L	L	L	L	L	L	L	L	H	64	H	1	1	1
L	L	L	L	L	L	L	H	L	64	H	2	2	1
L	L	L	L	L	L	H	L	L	64	H	4	4	1
L	L	L	L	L	H	L	L	L	64	H	8	8	1
L	L	L	L	H	L	L	L	L	64	H	16	16	1
L	L	L	H	L	L	L	L	L	64	H	32	32	1
L	L	L	H	H	H	H	H	H	64	H	63	63	1
L	L	L	H	H	H	H	H	H	64	L	H	63	1
L	L	L	H	L	H	L	L	L	64	H	40	40	1

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	120	mA
I_{OH}	MAX	16	mA
I_{OL}	MAX	-0.4	mA

SWITCHING CHARACTERISTICS

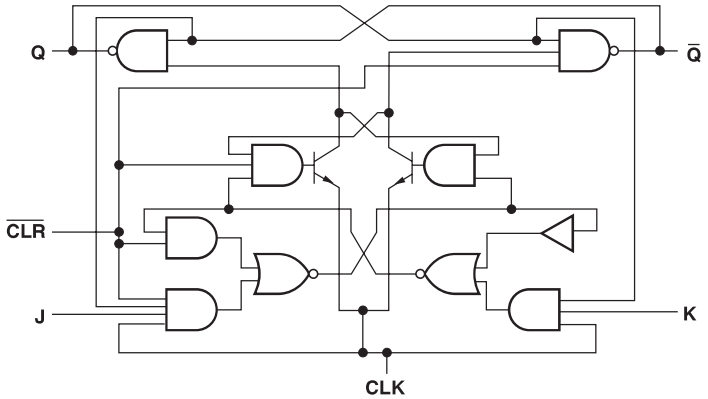
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL
fmax		A	QA	MIN	25
tw	CLK			MIN	20
	CLR			MIN	15
tsu	Positive			MIN	25
	Negative			MIN	0
th	Positive			MIN	0
	Negative			MIN	20
t_{PLH}		ENABLE	ENABLE	MAX	20
t_{PHL}				MAX	21
t_{PLH}		STRB	Z	MAX	18
t_{PHL}				MAX	23
t_{PLH}		CLK	Y	MAX	39
t_{PHL}				MAX	30
t_{PLH}		CLK	Z	MAX	18
t_{PHL}				MAX	26
t_{PLH}		RATE	Z	MAX	10
t_{PHL}				MAX	14
t_{PLH}		UNITY /CAS	Y	MAX	14
t_{PHL}				MAX	10
t_{PLH}		STRB	Y	MAX	30
t_{PHL}				MAX	33
t_{PLH}		CLK	ENABLE	MAX	30
t_{PHL}				MAX	33
t_{PLH}		CLR	Y	MAX	36
t_{PHL}			Z	MAX	23
t_{PLH}		RATE	Y	MAX	23
t_{PHL}				MAX	23

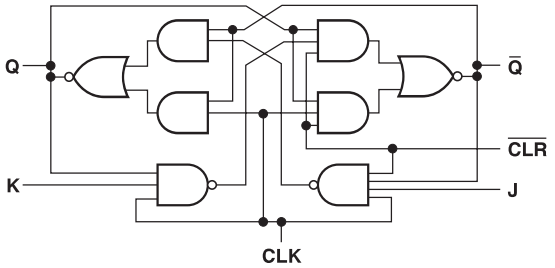
UNIT : fmax : MHz, other : ns

107

DUAL J-K FLIP-FLOPS WITH CLEAR

Logic Diagram





FUNCTION TABLES

'107

INPUTS				OUTPUTS	
$\overline{CLEAR}$	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍⎍	H	L	H	L
H	⎍⎍	L	H	L	H
H	⎍⎍	H	H	TOGGLE	

'LS107A,'HC107

INPUTS				OUTPUTS	
$\overline{CLEAR}$	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	20	6	0.04	0.08	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

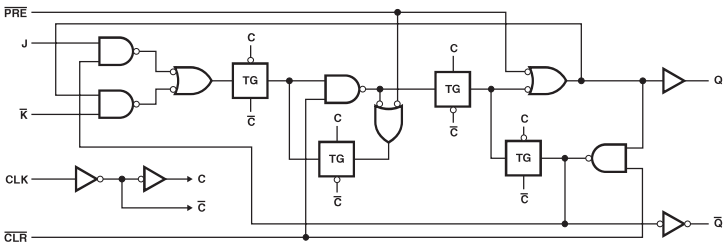
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HC
fmax				MIN	15	30	25	20	19
tw	CLK H			MIN	20	20	20	-	-
	CLK L			MIN	47	-	20	-	-
	$\overline{CP}$			MIN	-	-	-	24	27
	$\overline{CLR}$ L (or $\overline{R}$)			MIN	25	25	20	25	36
tsu	J, K			MIN	0	20	25	30	30
	$\overline{CLR}$ INACTIVE			MIN	0	25	25	-	-
th				MIN	0	0	0	3	5
t_{PLH}		$\overline{CLR}$ (or $\overline{R}$)	$\overline{Q}$	MAX	25	20	39	47	57
t_{PHL}			Q	MAX	40	20	39	47	57
t_{PLH}		CLK	$\overline{Q}$	MAX	25	20	32	-	-
t_{PHL}			Q	MAX	40	20	32	-	-
t_{PLH}		$\overline{CP}$	Q	MAX	-	-	-	51	65
t_{PHL}				MAX	-	-	-	51	65
t_{PLH}		$\overline{CP}$	$\overline{Q}$	MAX	-	-	-	51	60
t_{PHL}				MAX	-	-	-	51	60

UNIT fmax : MHz, other : ns

109

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRESET}$	$\overline{CLEAR}$	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_O	$\overline{Q}_O$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_O	$\overline{Q}_O$

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	15	8	4	17	17	0.04	0.08	0.08	0.08	0.08	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	16	4	8	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

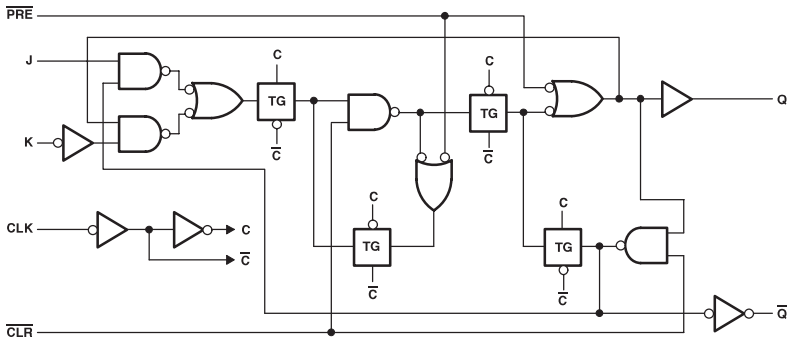
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax				MIN	25	25	34	105	90	25	25	19	100	100
tw	CLK H			MIN	20	25	14.5	4	4	20	-	-	-	-
	CLK L			MIN	20	-	14.5	5.5	5	20	-	-	-	-
	$\overline{CP}$			MIN	-	-	-	-	-	-	24	27	5	5
	$\overline{PRE}$ L			MIN	20	25	15	4	4	25	-	-	-	-
	$\overline{CLR}$ L			MIN	20	25	15	4	4	25	-	-	-	-
	$\overline{R}$			MIN	-	-	-	-	-	-	24	36	4.5	5.5
tsu	J, K			MIN	10	25	15	5.5	3	25	-	-	-	-
	$\overline{PRE}$, $\overline{CLR}$			MIN	10	-	10	2	2	6	-	-	-	-
	J, K to $\overline{CP}$			MIN	-	-	-	-	-	-	30	30	5.5	5.5
th				MIN	6	5	0	0	1	0	3	5	0	1
t_{PLH}		$\overline{PRE}$	Q	MAX	15	25	13	8	8	58	-	-	-	-
t_{PHL}			$\overline{Q}$	MAX	35	40	15	10.5	10.5	58	-	-	-	-
t_{PLH}		$\overline{CLR}$	$\overline{Q}$	MAX	15	25	13	8	8	58	-	-	-	-
t_{PHL}			Q	MAX	25	40	15	10.5	10.5	58	-	-	-	-
t_{PLH}		CLK	$\overline{Q}$,Q	MAX	16	25	16	9	8	44	-	-	-	-
t_{PHL}				MAX	28	40	18	9	9.2	44	-	-	-	-
t_{PLH}		$\overline{CP}$	Q	MAX	-	-	-	-	-	-	51	65	10.3	10.3
t_{PHL}				MAX	-	-	-	-	-	-	51	65	10.3	10.3
t_{PLH}		$\overline{CP}$	$\overline{Q}$	MAX	-	-	-	-	-	-	51	60	10.3	10.3
t_{PHL}				MAX	-	-	-	-	-	-	51	60	10.3	10.3
t_{PLH}		$\overline{R}$	$\overline{Q}$,Q	MAX	-	-	-	-	-	-	47	57	12.2	12.2
t_{PHL}				MAX	-	-	-	-	-	-	47	57	12.2	12.2

UNIT fmax : MHz, other : ns

112

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{CLEAR}$	A1	A2	B	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H	⎍⎍	⎍⎍
H	L	X	H	↑	⎍⎍	⎍⎍
H	X	L	↑	H	⎍⎍	⎍⎍
H	X	L	H	↑	⎍⎍	⎍⎍
H	H	↓	H	H	⎍⎍	⎍⎍
H	↓	↓	H	H	⎍⎍	⎍⎍
H	↓	H	H	H	⎍⎍	⎍⎍
↑	L	X	H	H	⎍⎍	⎍⎍
↑	X	L	H	H	⎍⎍	⎍⎍

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LVC 3V	UNIT
I_{CC}	MAX	6	25	4.5	19	0.04	0.08	0.08	0.08	0.08	0.01	mA
I_{OH}	MAX	-0.4	-1	-0.4	-1	-4	-4	-4	-24	-24	-24	mA
I_{OL}	MAX	8	20	8	20	4	4	4	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LVC 3V
fmax				MIN	30	80	30	100	20	20	20	150
tw	$\overline{PRE}$, $\overline{CLR}$			MIN	25	8	10	5	25	24	27	-
	CLK H			MIN	20	6	16.5	5	25	-	-	3.3
	CLK L			MIN	-	6.5	16.5	5	25	-	-	3.3
	$\overline{CP}$			MIN	-	-	-	-	-	24	24	-
tsu	DATA			MIN	20	7	22	5	25	24	24	2.3
	$\overline{PRE}$ INACTIVE			MIN	25	-	20	5	25	-	-	2.4
	$\overline{CLR}$ INACTIVE			MIN	20	-	20	5	25	-	-	2.4
th				MIN	0	0	0	0	0	0	3	0.7
t_{PLH}		$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	MAX	20	7	15	7.5	41	-	-	4.8
t_{PHL}				MAX	20	7	18	7.5	41	-	-	4.8
t_{PLH}		CLK	Q or $\overline{Q}$	MAX	20	7	15	7.5	31	-	-	5.9
t_{PHL}				MAX	20	7	19	7.5	31	-	-	5.9
t_{PLH}		$\overline{CP}$	Q or $\overline{Q}$	MAX	-	-	-	-	-	53	53	-
t_{PHL}				MAX	-	-	-	-	-	53	53	-
t_{PLH}		$\overline{S}$	Q or $\overline{Q}$	MAX	-	-	-	-	-	47	48	-
t_{PHL}				MAX	-	-	-	-	-	47	48	-
t_{PLH}		$\overline{R}$	Q or $\overline{Q}$	MAX	-	-	-	-	-	54	56	-
t_{PHL}				MAX	-	-	-	-	-	54	56	-

UNIT fmax : MHz, other : ns

121

MONOSTABLE MULTIVIBRATOR

- Internal Timing Resistors (2kΩ)
- Programmable Output Pulse Width with Rext/Cext: 40ns to 28s

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L†	H†
X	X	L	L†	H†
H	H	X	L†	H†
H	↓	H	⎍⎍	⎍⎍
↓	H	H	⎍⎍	⎍⎍
↓	↓	H	⎍⎍	⎍⎍
L	X	↑	⎍⎍	⎍⎍
X	L	↑	⎍⎍	⎍⎍

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

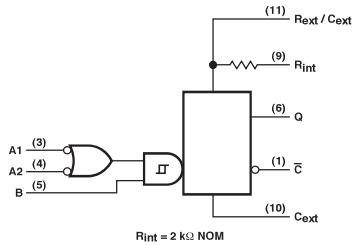
PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	40	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tw (IN)			MIN	50
t_{PLH}	A	Q	MAX	70
t_{PHL}	B			80
t_{PLH}	A	$\overline{Q}$	MAX	55
t_{PHL}	B			65

UNIT: NS

Logic Diagram



R_{int} = 2 kΩ NOM

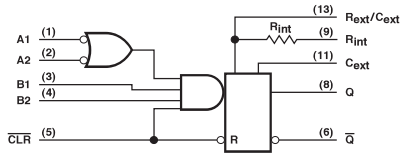
NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repetability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

122

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle
- Internal Timing Resistors (5kΩ)

Logic Diagram



R_{int} is nominally 10 kW for '122 and 'LS122

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{CLEAR}$	A1	A2	B	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H	⎍⎍	⎍⎍
H	L	X	H	↑	⎍⎍	⎍⎍
H	X	L	↑	H	⎍⎍	⎍⎍
H	X	L	H	↑	⎍⎍	⎍⎍
H	H	↓	H	H	⎍⎍	⎍⎍
H	↓	↓	H	H	⎍⎍	⎍⎍
H	↓	H	H	H	⎍⎍	⎍⎍
↑	L	X	H	H	⎍⎍	⎍⎍
↑	X	L	H	H	⎍⎍	⎍⎍

See explanation of function table on page
† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	66	11	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_W			MIN	40	40
t_{PLH}	A	Q	MAX	33	33
	B			28	44
t_{PHL}	A	$\overline{Q}$	MAX	40	45
	B			36	56
t_{PLH}	CLEAR	Q	MAX	27	27
t_{PHL}		$\overline{Q}$		40	45

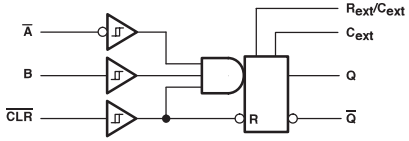
UNIT: NS

123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBARATORS WITH CLEAR

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	$\overline{A}$ (A)	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍⎍	⎍⎍
H	↓	H	⎍⎍	⎍⎍
↑	L	H	⎍⎍	⎍⎍

See explanation of function table on page
† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	66	20	0.16	0.16	0.65	0.975	0.28	0.65	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-8	-8	-6	-12	mA
I_{OL}	MAX	16	8	4	4	8	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
t_W			MIN	40	40	30	30	5	5	5	5
t_{PLH}	$\overline{A}$ (A)	Q	MAX	33	33	90	-	16	12	27.5	16
	B			28	44	90	-	16	12	27.5	16
t_{PHL}	$\overline{A}$ (A)	$\overline{Q}$	MAX	40	45	96	-	16	12	27.5	16
	B			36	56	96	-	16	12	27.5	16
t_{PLH}	$\overline{CLEAR}$ (R)	Q	MAX	27	27	65	-	13	14	22	13
t_{PHL}		$\overline{Q}$		40	45	65	-	13	14	22	13

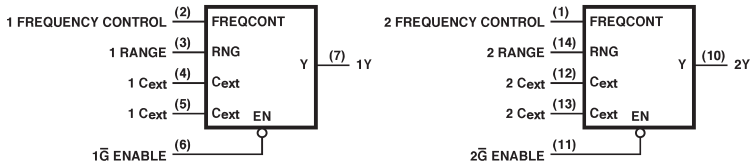
UNIT: NS

124

DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS

- Frequency Spectrum: 1Hz to 60MHz
- Typical fmax: 85MHz
- Typical Power Dissipation: 525mW

Block Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	UNIT
I_{CC}	MAX	150	mA
I_{OH}	MAX	-1	mA
I_{OL}	MAX	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	S
f_O	MIN	60

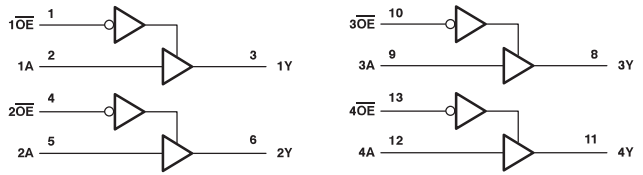
UNIT: NS

125

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

- Y = A

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	UNIT
I_{CC}	MAX	54	20	40	0.08	0.16	0.08	0.16	49	49	30	mA
I_{OH}	MAX	-5.2	-2.6	-15	-6	-6	-6	-6	-15	-15	-32	mA
I_{OL}	MAX	16	24	64	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
I_{CC}	MAX	7	0.04	0.02	0.02	0.02	0.01	0.01	mA
I_{OH}	MAX	-32	-8	-8	-8	-16	-24	-24	mA
I_{OL}	MAX	64	8	8	8	16	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT
t_{PLH}	A	Y	MAX	13	15	6.5	30	30	33	38	5.7	6	4.9
t_{PHL}			MAX	18	18	8	30	30	33	38	7.7	8	4.9
t_{PZH}	$\overline{G}$	Y	MAX	17	20	8.5	30	38	35	38	10.3	11.1	5.9
t_{PZL}			MAX	25	25	9	30	38	35	38	11.7	12.8	6.8
t_{PHZ}			MAX	8	20	6	30	38	33	42	8.9	9.4	6.2
t_{PLZ}			MAX	12	20	6	30	38	33	42	8.6	9.9	6.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC
t_{PLH}	A	Y	MAX	3.5	8.5	8.5	13	8.5	4.8	2.8
t_{PHL}			MAX	3.9	8.5	8.5	13	8.5	4.8	2.8
t_{PZH}	$\overline{G}$	Y	MAX	4	8	8	13	8	5.4	3.5
t_{PZL}			MAX	4	8	8	13	8	5.4	3.5
t_{PHZ}			MAX	4.5	10	10	15	10	4.6	4
t_{PLZ}			MAX	4.5	10	10	15	10	4.6	4

UNIT: NS

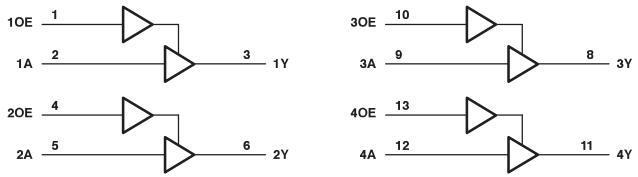
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

126

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

● Y = A

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVTH 3V	UNIT
I_{CC}	MAX	62	22	48	0.08	0.16	0.16	51	51	30	7	mA
I_{OH}	MAX	-5.2	-2.6	-15	-6	-6	-6	-15	-15	-32	-32	mA
I_{OL}	MAX	16	24	64	6	6	6	64	64	64	64	mA

PARAMETER	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
I_{CC}	MAX	0.04	0.02	0.02	0.02	0.01	0.01	mA
I_{OH}	MAX	-8	-8	-8	-16	-24	-24	mA
I_{OL}	MAX	8	8	8	16	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVTH 3V
t_{PLH}	A	Y	MAX	13	15	7	30	30	36	6.3	6.3	6.3	3.8
t_{PHL}			MAX	18	18	8.5	30	30	36	7.4	7.4	5.7	3.9
t_{PZH}	G	Y	MAX	18	25	8.5	30	38	38	7.9	7.9	6.5	5.4
t_{PZL}			MAX	25	35	8.5	30	38	38	10.5	10.5	6.5	5.2
t_{PHZ}			MAX	16	25	7.5	30	38	42	10	10	6.8	3.8
t_{PLZ}			MAX	18	25	8	30	38	42	12.3	12.3	6.7	5.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 5V	LV 3V	LVC 3V	ALVC
t_{PLH}	A	Y	MAX	8.5	8.5	8.5	13	4.7	3.1
t_{PHL}			MAX	8.5	8.5	8.5	13	4.7	3.1
t_{PZH}	G	Y	MAX	8	8	8	13	5.7	3.3
t_{PZL}			MAX	8	8	8	13	5.7	3.3
t_{PHZ}			MAX	10	10	10	15	6	3.7
t_{PLZ}			MAX	10	10	10	15	6	3.7

UNIT: ns

128

50-Ω LINE DRIVERS

● Y = $\overline{A + B}$

Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	57	mA
I_{OH}	MAX	-42.4	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A, B	Y	MAX	9
t_{PHL}	A, B	Y	MAX	12

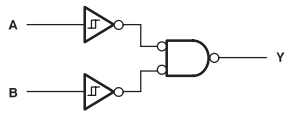
UNIT: ns

132

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

● Y = $\overline{A \bullet B}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	40	14	68	0.02	0.04	0.04	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-1	-4	-4	-4	-8	-8	-6	-12	mA
I_{OL}	MAX	16	8	20	4	4	4	8	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
t_{PLH}	A, B	Y	MAX	22	22	10.5	31	38	50	11	10	17.5	11
t_{PHL}	A, B	Y	MAX	22	22	13	31	38	50	11	8	17.5	11

UNIT: ns

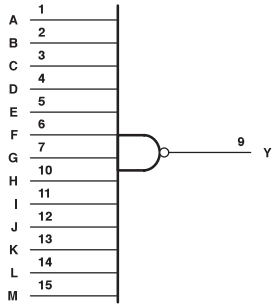
▭ : **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

133

13-INPUT POSITIVE-NAND GATES

● $Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H \bullet I \bullet J \bullet K \bullet L \bullet M}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	ALS	SN74 HC	UNIT
I_{CC}	MAX	10	0.34	0.02	mA
I_{OH}	MAX	-1	-0.4	-4	mA
I_{OL}	MAX	20	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	ALS	SN74 HC
t_{PLH}	A to M	Y	MAX	6	11	38
t_{PHL}	A to M	Y	MAX	7	25	38

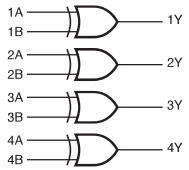
UNIT: ns

136

QUAD EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

● $Y = A \oplus B = \overline{A}B + A\overline{B}$

Logic Diagram



FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	UNIT
I_{CC}	MAX	50	10	5.9	31	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	16	8	8	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS
t_{PLH}	A or B	Y (Other Output = L)	MAX	18	30	50	12.5
t_{PHL}	A or B	Y (Other Output = L)	MAX	50	30	15	7.1
t_{PLH}	A or B	Y (Other Output = L)	MAX	22	30	50	11.4
t_{PHL}	A or B	Y (Other Output = L)	MAX	55	30	15	10.7

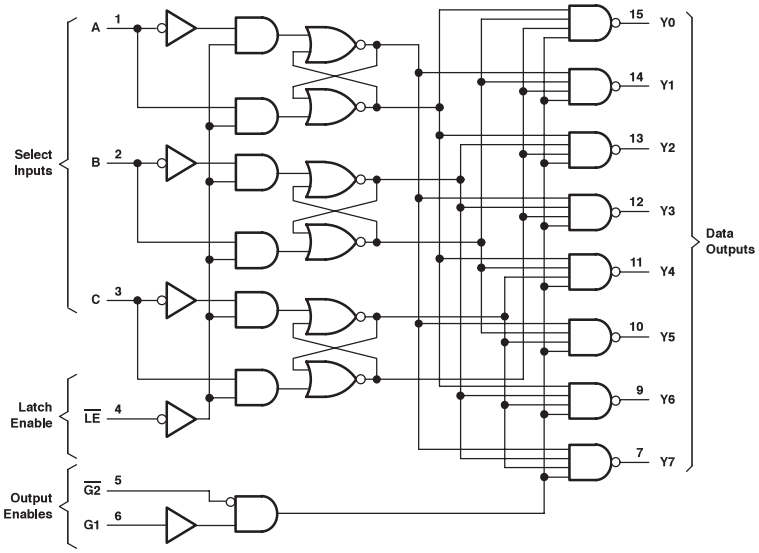
UNIT: ns

137

3-TO-8 LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

● Incorporates Two Output Enables To Simplify Cascading

Logic Diagram



▭ : OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{LE}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
I_{CC}	MAX	18	11	24	0.08	0.16	0.08	0.16	mA
I_{OH}	MAX	-0.4	-0.4	-2	-4	-4	-4	-4	mA
I_{OL}	MAX	8	8	20	4	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t_{PLH}	A, B, C	Y (CD74: $\overline{Y}$)	MAX	24	20	12.5	48	54	48	57
t_{PHL}			MAX	38	20	12.5	48	54	48	57
t_{PLH}	$\overline{G2}$	Y (CD74: $\overline{Y}$)	MAX	21	12	8	36	44	36	56
t_{PHL}			MAX	27	15	8.5	36	44	36	56
t_{PLH}	G1	Y (CD74: $\overline{Y}$)	MAX	21	17	10	36	44	36	53
t_{PHL}			MAX	27	15	9	36	44	36	53
t_{PLH}	$\overline{LE}$ (CD74: LE)	Y (CD74: $\overline{Y}$)	MAX	27	22	13.5	48	57	52	66
t_{PHL}			MAX	38	20	14	48	57	52	66

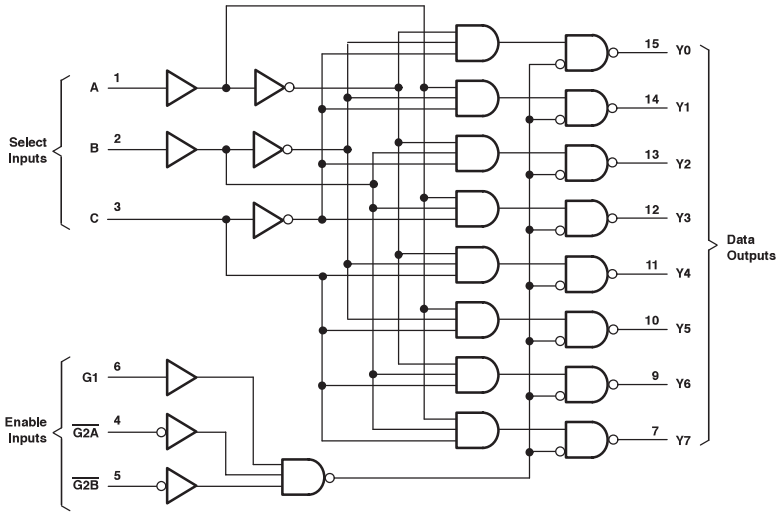
UNIT:ns

138

3-TO-8 LINE DECODERS/DEMULTIPLEXRS

- 3 Enable Inputs to Simplify Cascading and /or Data Reception
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

$\overline{G2}$* = $\overline{G2A}$•$\overline{G2B}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	UNIT
I_{CC}	MAX	10	74	10	20	20	0.08	0.16	0.08	0.16	0.04	mA
I_{OH}	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	mA
I_{OL}	MAX	8	20	8	20	20	4	4	4	4	24	mA

PARAMETER	MAX or MIN	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.16	0.04	0.16	0.04	0.04	0.02	0.02	0.01	mA
I_{OH}	MAX	-24	-24	-24	-8	-8	-6	-12	-24	mA
I_{OL}	MAX	24	24	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11
t_{PLH}	A, B, C	Y (CD74:$\overline{Y}$)	MAX	27	12	22	10	8.5	45	45	45	53	8.1
t_{PHL}			MAX	39	12	18	9.5	9	45	45	45	53	8.8
t_{PLH}	$\overline{G2}$	Y (CD74:$\overline{Y}$)	MAX	26	11	17	7.5	8	39	53	42	53	8.3
t_{PHL}			MAX	38	11	17	8.5	7.5	39	53	42	53	8.3
t_{PLH}	G1	Y (CD74:$\overline{Y}$)	MAX	26	11	17	10	9	39	53	42	53	7.5
t_{PHL}			MAX	38	11	17	10	8.5	39	53	42	53	7.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	A, B, C	Y (CD74:$\overline{Y}$)	MAX	11	9.8	12	11.5	13	18	11.5	6.7
t_{PHL}			MAX	11	9.7	12	11.5	13	18	11.5	6.7
t_{PLH}	$\overline{G2}$	Y (CD74:$\overline{Y}$)	MAX	10	8.9	10.5	11.5	12	18	11.5	6.5
t_{PHL}			MAX	10	8.9	10.5	11.5	12	18	11.5	6.5
t_{PLH}	G1	Y (CD74:$\overline{Y}$)	MAX	11	9.3	11	11.5	11.5	18.5	11.5	5.8
t_{PHL}			MAX	11	9.8	11	11.5	11.5	18.5	11.5	5.8

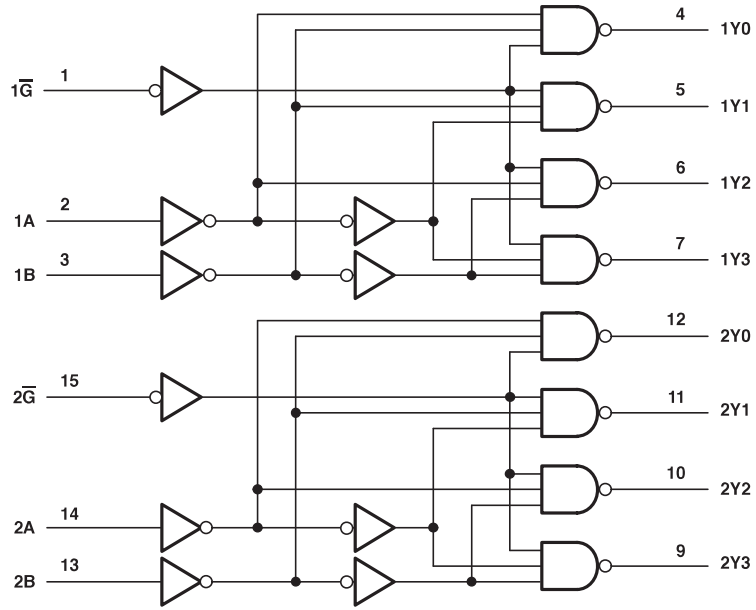
UNIT: ns

139

DUAL 2-TO-4-LINE DECODERS/DEMULTIPLEXERS

- Incorporate Two Enable Inputs to Simplify Cascading and /or Data Reception
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11	CD74 ACT	UNIT
I_{CC}	MAX	11	90	13	0.08	0.08	0.08	0.16	0.16	0.08	0.16	mA
I_{OH}	MAX	-0.4	-1	-0.4	-4	-4	-4	-4	-24	-24	-24	mA
I_{OL}	MAX	8	20	8	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.04	0.02	-	0.02	0.01	mA
I_{OH}	MAX	-8	-8	-6	-12	-24	mA
I_{OL}	MAX	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11	CD74 ACT
t_{PLH}	A or B	Y (CD74: $\overline{Y}$)	MAX	29	12	14	44	44	43	51	10.5	8.5	11.5
t_{PHL}	A or B	Y (CD74: $\overline{Y}$)	MAX	38	12	14	44	44	43	51	10.5	8.5	11.5
t_{PLH}	G	Y (CD74: $\overline{Y}$)	MAX	24	8	14	44	41	43	51	10.5	7.9	12
t_{PHL}	G	Y (CD74: $\overline{Y}$)	MAX	32	10	15	44	41	43	51	10.5	7.5	12

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	A or B	Y (CD74: $\overline{Y}$)	MAX	10.5	10.5	16.5	10.5	6.2
t_{PHL}	A or B	Y (CD74: $\overline{Y}$)	MAX	10.5	10.5	16.5	10.5	6.2
t_{PLH}	G	Y (CD74: $\overline{Y}$)	MAX	9.5	9.5	14.5	9.5	4.7
t_{PHL}	G	Y (CD74: $\overline{Y}$)	MAX	9.5	9.5	14.5	9.5	4.7

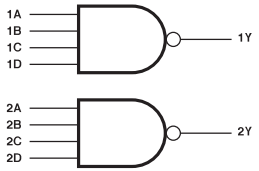
UNIT: ns

140

DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

● $Y = \overline{ABCD}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	UNIT
I_{CC}	MAX	44	mA
I_{OH}	MAX	-40	mA
I_{OL}	MAX	60	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S
t_{PLH}	A, B, C, D	Y	MAX	6.5
t_{PHL}			MAX	6.5

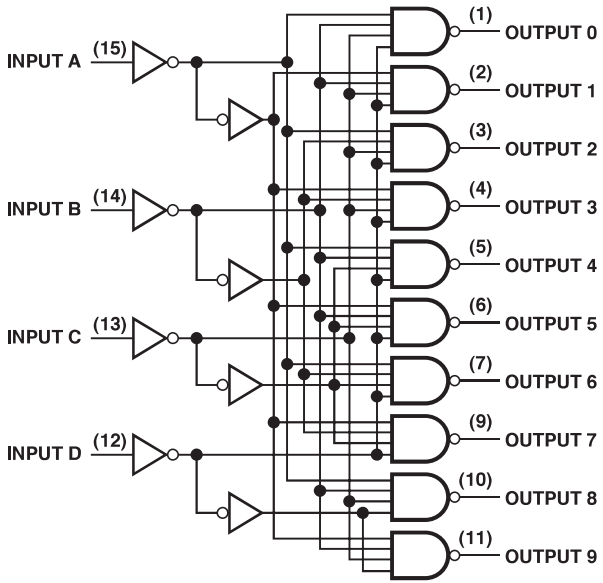
UNIT: ns

145

BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS

- Sink-Current Capability: 80mA
- Low Power Dissipation (SN74LS): 35mW (typ)

Logic Diagram



FUNCTION TABLE

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	70	13	mA
V_O (OFF)	MAX	15	15	mA

SWITCHING CHARACTERISTICS

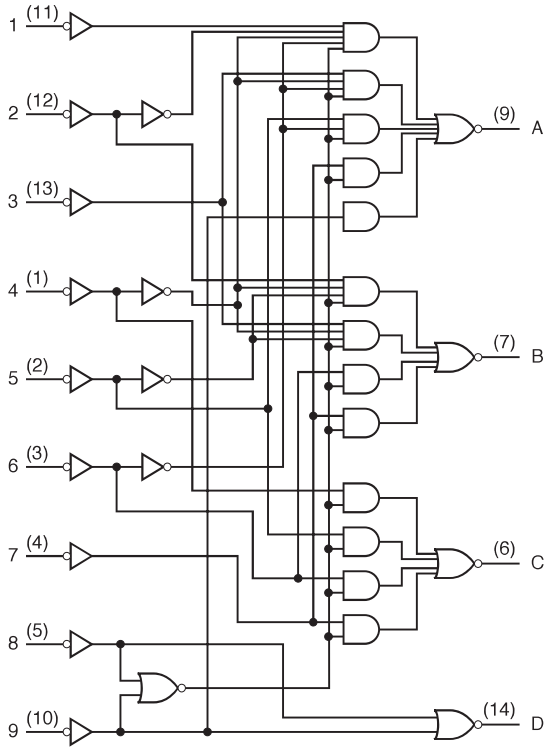
PARAMETER	MAX or MIN	TTL	LS
t_{PLH}	MAX	50	50
t_{PHL}	MAX	50	50

UNIT: ns

147

10-TO-4 LINE PRIORITY ENCODER

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	70	20	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

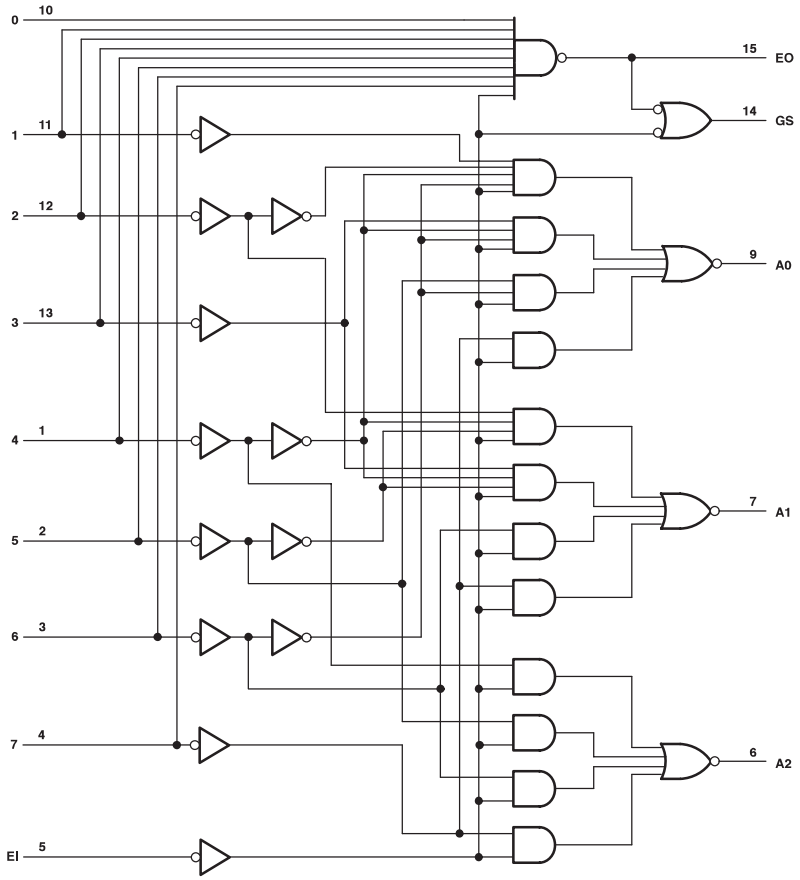
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	MAX	19	33	48	48	53
t_{PHL}	MAX	19	23	48	48	53

UNIT:ns

148

8-TO 3-LINE OCTAL PRIORITY ENCODERS

Logic Diagram



FUNCTION TABLE

INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	UNIT
I_{CC}	MAX	60	20	0.08	mA
I_{OL}	MAX	16	8	4	mA
I_{OH}	MAX	-0.8	-0.4	-4	mA

SWITCHING CHARACTERISTICS

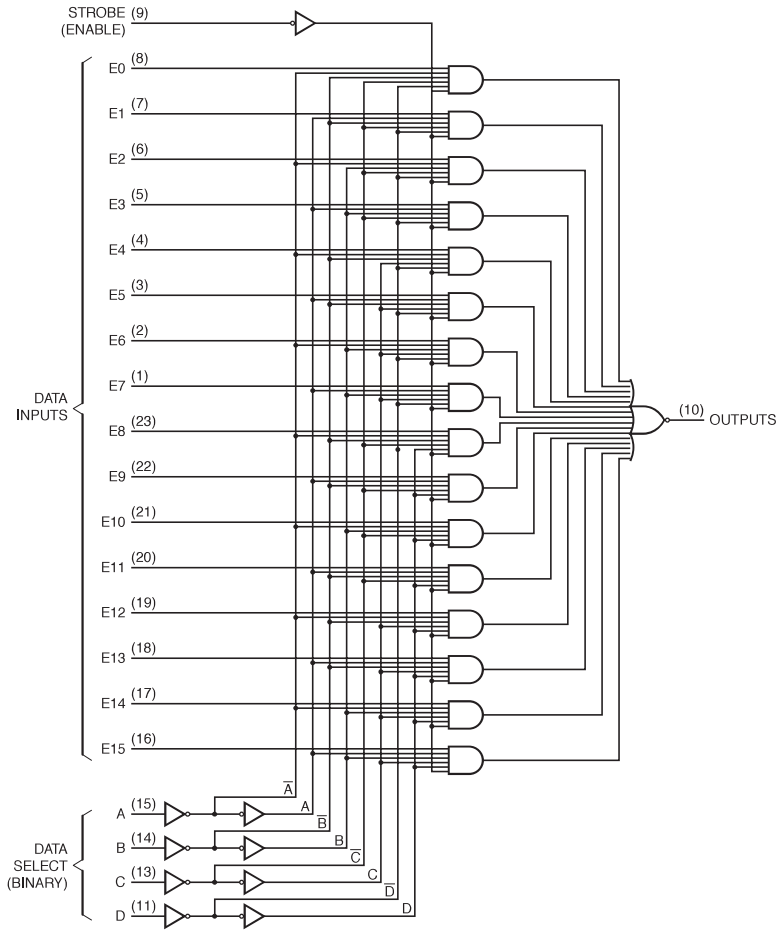
PARAMETER	INPUT	OUTPUT	WAVEFORM	MAX or MIN	TTL	LS	SN74 HC
t_{PLH}	1 to 7	A0, A1 or A2	In-phase output	MAX	15	18	45
t_{PHL}					14	25	45
t_{PLH}	1 to 7	A0, A1 or A2	Out-of-phase output	MAX	19	36	45
t_{PHL}					19	29	45
t_{PLH}	0 to 7	EO	Out-of-phase output	MAX	10	18	38
t_{PHL}					25	40	38
t_{PLH}	0 to 7	GS	In-phase output	MAX	30	55	48
t_{PHL}					25	21	48
t_{PLH}	E1	A0, A1 or A2	In-phase output	MAX	15	25	49
t_{PHL}					15	25	49
t_{PLH}	E1	GS	In-phase output	MAX	12	17	36
t_{PHL}					15	36	36
t_{PLH}	E1	EO	In-phase output	MAX	15	21	41
t_{PHL}					30	35	41

UNIT: ns

150

1-OF-16 DATA SELECTOR

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
SELECT				STROBE	
D	C	B	A	$\overline{G}$	W
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

NOTES:
H = High Level, L = Low Level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ ... $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 ... D7 = the level of the D respective input

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	48	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

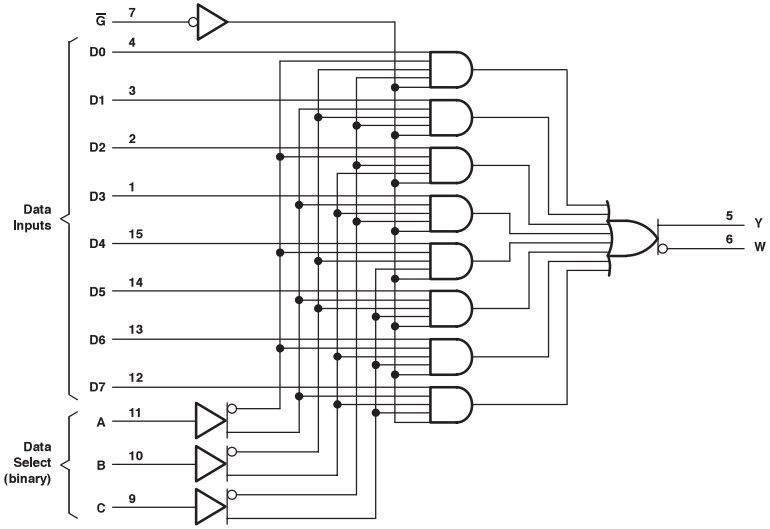
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A, B, C or D	W	MAX	35
t_{PHL}				33
t_{PLH}	Strobe $\overline{G}$	W	MAX	24
t_{PHL}				30
t_{PLH}	E0 thru E15 or E0 thru D7	W	MAX	14
t_{PHL}				20

UNIT:ns

151

8-TO-1 LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT					
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	48	10	70	12	30	21	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	24	48	24	6	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A, B or C	Y	MAX	38	43	18	18	14.5	12	63	56	62
t_{PHL}				38	30	18	24	15	9	63	56	62
t_{PLH}	A, B or C	W (CD74: $\overline{Y}$)	MAX	26	23	15	24	12	9.5	63	62	65
t_{PHL}				30	32	13.5	23	12	7.5	63	62	65
t_{PLH}	D0 to D7	Y	MAX	20	32	16.5	10	10.5	7.5	49	51	57
t_{PHL}				27	26	18	15	11	7.5	49	51	57
t_{PLH}	D0 to D7	W (CD74: $\overline{Y}$)	MAX	14	21	13	15	6.5	7	49	56	54
t_{PHL}				14	20	12	15	4.5	5	49	56	54
t_{PLH}	$\overline{G}$	Y	MAX	33	42	12	18	14	10.5	32	42	44
t_{PHL}				33	32	12	19	11	7.5	32	42	44
t_{PLH}	$\overline{G}$	W (CD74: $\overline{Y}$)	MAX	21	24	7	19	6	7	32	44	54
t_{PHL}				23	30	7	23	10	6	32	44	54

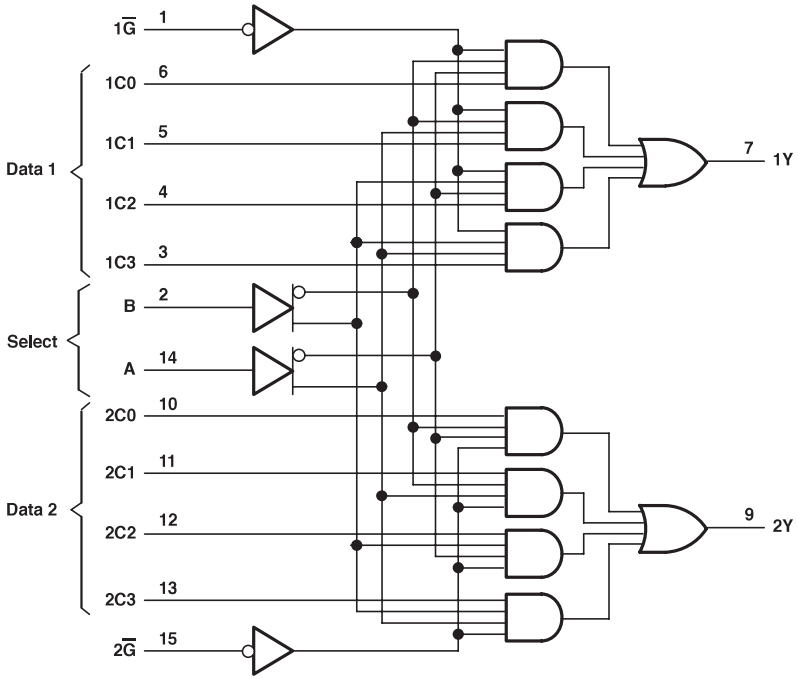
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT
t_{PLH}	A, B or C	Y	MAX	18.2	20.2
t_{PHL}				18.2	20.2
t_{PLH}	A, B or C	W (CD74: $\overline{Y}$)	MAX	19.6	21.6
t_{PHL}				19.6	21.6
t_{PLH}	D0 to D7	Y	MAX	13.5	15.5
t_{PHL}				13.5	15.5
t_{PLH}	D0 to D7	W (CD74: $\overline{Y}$)	MAX	14.9	16.9
t_{PHL}				14.9	16.9
t_{PLH}	$\overline{G}$	Y	MAX	12.2	12.1
t_{PHL}				12.2	12.1
t_{PLH}	$\overline{G}$	W (CD74: $\overline{Y}$)	MAX	13.5	13.5
t_{PHL}				13.5	13.5

UNIT: ns

153

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUTS
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	60	10	70	14	33	20	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	24	48	20	6	4	4	24	24	mA

SWITCHING CHARACTERISTICS

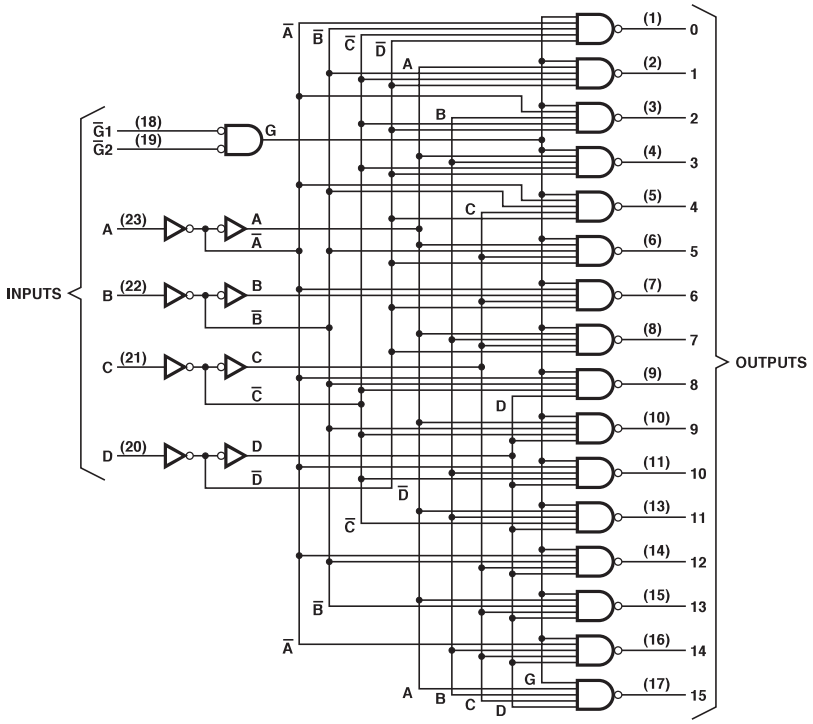
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	DATA	Y	MAX	18	15	9	10	7	8	35	44	51	13.3	18
t_{PHL}			MAX	23	26	9	15	8	7.5	35	44	51	13.3	18
t_{PLH}	SELECT	Y	MAX	34	29	18	21	12.5	12	38	48	51	20	22
t_{PHL}			MAX	34	38	18	21	11	10.5	38	48	51	20	22
t_{PLH}	STROBE	Y	MAX	30	24	15	18	11.5	10.5	24	36	41	11.8	12.6
t_{PHL}			MAX	23	32	13.5	18	9	8	24	36	41	11.8	12.6

UNIT: ns

154

4-LINE TO 16-LINE DECODER/DEMULTIPLEXER

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS													
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	56	23	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	24	-4	-4	-4	mA
I_{OL}	MAX	16	-0.4	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A, B, C, D	0 to 15 ($\overline{Y}$) (CD74: Y0 to $\overline{Y15}$)	MAX	36	12	45	53	53
t_{PHL}				33	12	45	53	53
t_{PLH}	G1 to G2	0 to 15 ($\overline{Y}$) (CD74: Y0 to $\overline{Y15}$)	MAX	30	12	45	53	51
t_{PHL}				27	12	45	53	51

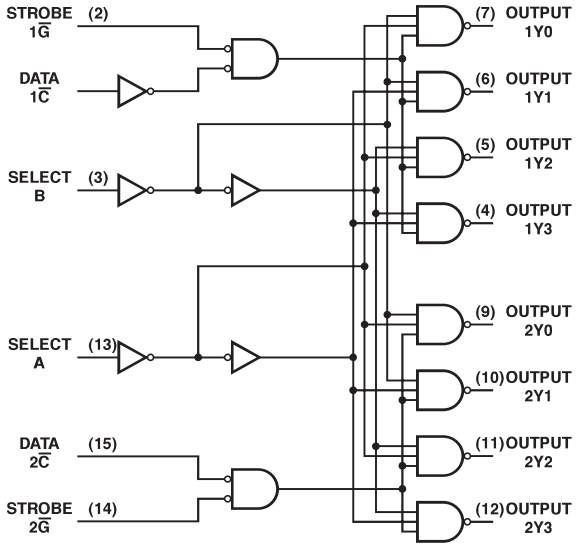
UNIT: ns

155

DECODERS/DEMULTIPLEXERS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Lager Words
- Outputs: Totem Pole

Logic Diagram



FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$\overline{1G}$	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$\overline{2G}$	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER OR
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE or DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	$\overline{G}$‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

† C = inputs 1C and $2\overline{C}$ connected together
‡ $\overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I_{CC}	MAX	40	10	13	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	mA
I_{OL}	MAX	16	8	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t_{PLH}	A or B	Y	MAX	32	26	14
t_{PHL}	A or B			32	30	12
t_{PLH}	1C	Y	MAX	24	27	12
t_{PHL}	1C			30	27	14

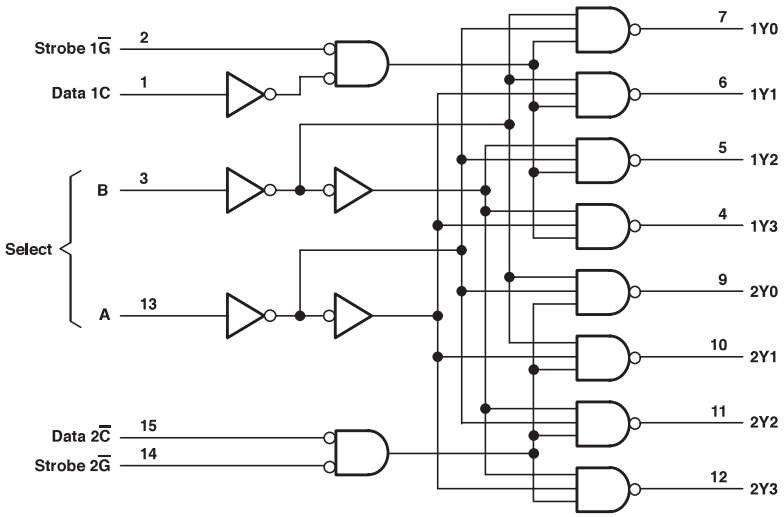
UNIT: ns

156

DECODERS/DEMULTIPLEXERS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Lager Words
- Outputs: Open-Collector

Logic Diagram



FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$1\overline{G}$	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$2\overline{G}$	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER OR
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE or DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	$\overline{G}$‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

† C = inputs 1C and $2\overline{C}$ connected together
‡ $\overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I_{CC}	MAX	40	10	9	mA
I_{OL}	MAX	16	8	8	mA
V_{OH}	MAX	5.5	5.5	5.5	mA

SWITCHING CHARACTERISTICS

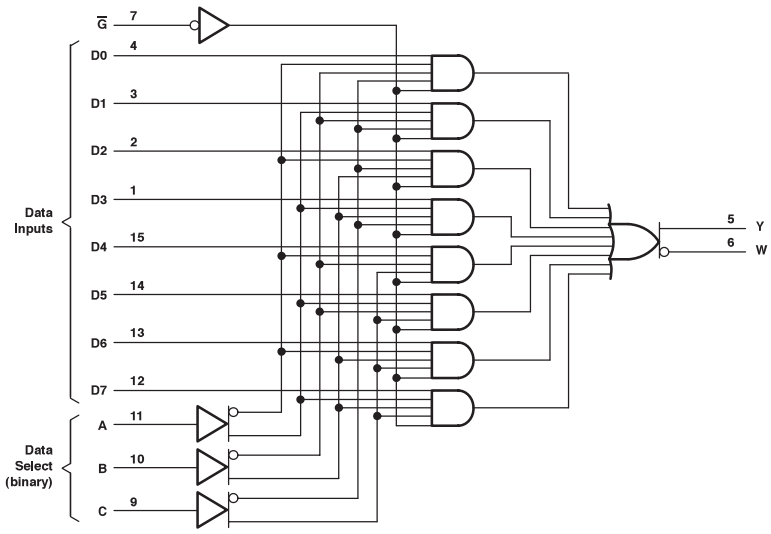
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t_{PLH}	$2\overline{C}$ or $1\overline{G}$ or $2\overline{G}$	Y	MAX	23	40	38
t_{PHL}				30	51	22
t_{PLH}	A or B	Y	MAX	34	46	55
t_{PHL}	A or B			34	51	25
t_{PLH}	1C	Y	MAX	27	48	50
t_{PHL}	1C			33	48	23

UNIT: ns

157

QUAD 2-TO-1 LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
I_{CC}	MAX	48	16	78	11	28	23	0.08	0.16	0.08	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-6	-4	-6	-4	mA
I_{OL}	MAX	16	8	20	8	20	20	6	4	6	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.16	0.16	0.04	0.02	-	0.0.2	0.01	mA
I_{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	mA
I_{OL}	MAX	24	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t_{PLH}	DATA	Y	MAX	14	14	7.5	14	6	6.5	32	38	35	38
t_{PHL}				14	14	6.5	12	5.5	7	32	38	35	38
t_{PLH}	STROBE	Y	MAX	20	20	12.5	20	10.5	11	29	41	33	41
t_{PHL}				21	21	12	13	7.5	7	29	41	33	41
t_{PLH}	SELECT	Y	MAX	23	23	15	24	11	11	31	44	40	44
t_{PHL}				27	27	15	17	10	8	31	44	40	44

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	DATA	Y	MAX	8.5	9.5	9.5	9.8	15	9.5	5.2
t_{PHL}				8.5	9.5	9.5	9.8	15	9.5	5.2
t_{PLH}	STROBE	Y	MAX	13.5	13.5	12	12	19.5	12	6.5
t_{PHL}				13.5	13.5	12	12	19.5	12	6.5
t_{PLH}	SELECT	Y	MAX	14.5	14.5	11.5	12	19	11.5	6.8
t_{PHL}				14.5	14.5	11.5	12	19	11.5	6.8

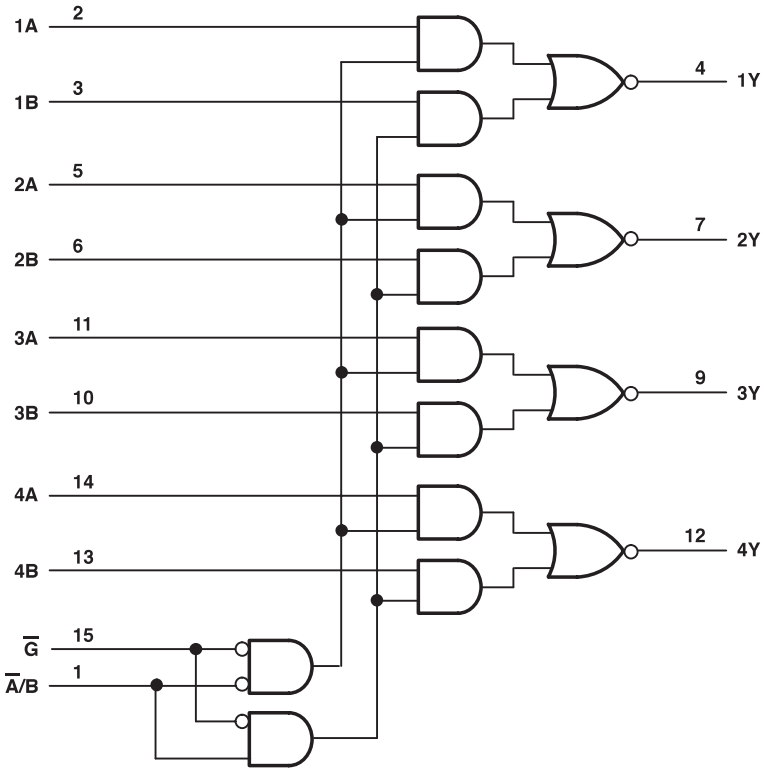
UNIT: ns

158

QUAD 2-TO-1 LINE DATA SLECTORS/MULTIPLEXERS

- Buffered Inputs and Outputs

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	11	81	10	22.5	15	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.4	-1	-0.4	-2	-1	-6	-4	-4	mA
I_{OL}	MAX	8	20	8	20	20	6	4	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	UNIT
I_{CC}	MAX	0.16	0.16	0.04	0.02	mA
I_{OH}	MAX	-24	-24	-8	-8	mA
I_{OL}	MAX	24	24	8	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	DATA	Y	MAX	12	6	15	5	7	32	42	42
t_{PHL}				15	6	8	4.5	4.5	32	42	42
t_{PLH}	STROBE	Y	MAX	17	11.5	18	6.5	7	29	48	48
t_{PHL}				24	12	18	10	6.5	29	48	48
t_{PLH}	SELECT	Y	MAX	20	12	18	9.5	9.5	31	45	45
t_{PHL}				24	12	18	10.5	7	31	45	45

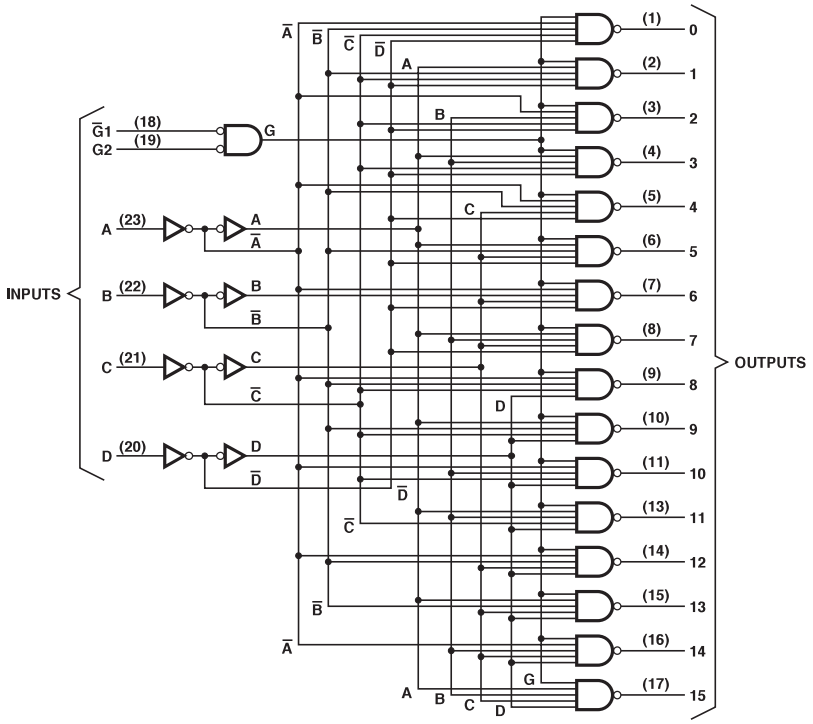
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT
t_{PLH}	DATA	Y	MAX	8	9.2	9.5	9.8
t_{PHL}				8	9.2	9.5	9.8
t_{PLH}	STROBE	Y	MAX	11.9	12.4	12	12
t_{PHL}				11.9	12.4	12	12
t_{PLH}	SELECT	Y	MAX	12.9	13.5	11.5	12
t_{PHL}				12.9	13.5	11.5	12

UNIT: ns

159

4-TO-16 LINE DECODER/DEMULTIPLEXER

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS													
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	56	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	INPUT	ANY	MAX	36
t_{PHL}				36
t_{PLH}	STROBE	ANY	MAX	25
t_{PHL}				36

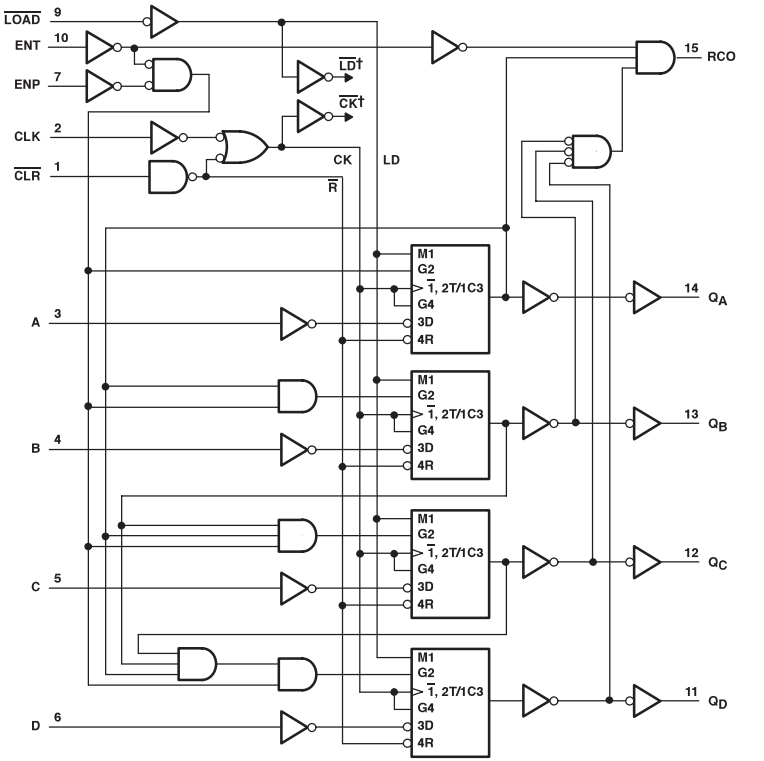
UNIT: ns

161

SYNCHRONOUS 4-BIT BINARY COUNTERS

- Asynchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	101	32	21	53	55	0.08	0.16	0.16	0.08	0.08	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	8	20	20	-4	4	4	24	24	-6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	40	75	90	25	20	20
tw	CLOCK			MIN	25	25	-	-	7	20	24	24
	CLEAR				20	20	15	8	5	20	30	30
tsu	INPUT A, B, C, D			MIN	20	20	15	8	5	38	18	15
	ENABLE, P, T				20	20	15	8	11.5	43	15	20
	LOAD				25	20	15	8	11.5	34	18	18
	CLEAR INACTIVE				20	25	10	8	-	31	20	-
th				MIN	0	3	0	0	2	0	3	5
t_{PLH}		CLOCK	RIPPLE CARRY	MAX	35	35	20	16.5	15	54	56	63
t_{PHL}					35	35	20	12.5	15	54	56	63
t_{PLH}		CLOCK	ANY Q	MAX	25	24	15	7	9.5	51	56	59
t_{PHL}					29	27	20	13	11	51	56	59
t_{PLH}		ENABLE T	RIPPLE CARRY	MAX	16	14	13	9	8.5	49	36	48
t_{PHL}					16	14	13	8.5	8.5	49	36	48
t_{PHL}		CLEAR	ANY Q	MAX	38	28	24	13	13	53	63	75
			RIPPLE CARRY	MAX	-	-	23	12.5	11.5	55	63	75

PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax				MIN	103	91	50	85
tw	CLOCK			MIN	4.8	5.4	5	5
	CLEAR				4.4	5.3	5	5
tsu	INPUT A, B, C, D			MIN	4.4	4.4	6.5	4.5
	ENABLE, P, T				-	-	9	6
	LOAD				5.3	5.3	9.5	6
	CLEAR INACTIVE				-	-	2.5	1.5
th				MIN	0	0	1	1
t_{PLH}		CLOCK	RIPPLE CARRY	MAX	15.2	15.2	23.5	14
t_{PHL}					15.2	15.2	23.5	14
t_{PLH}		CLOCK	ANY Q	MAX	15	15	18.5	11.5
t_{PHL}					15	15	18.5	11.5
t_{PLH}		ENABLE T	RIPPLE CARRY	MAX	9.4	9.8	18	11.5
t_{PHL}					9.4	9.8	18	11.5
t_{PHL}		CLEAR	ANY Q	MAX	15	15	19.5	12.5
			RIPPLE CARRY	MAX	15	15	19	12

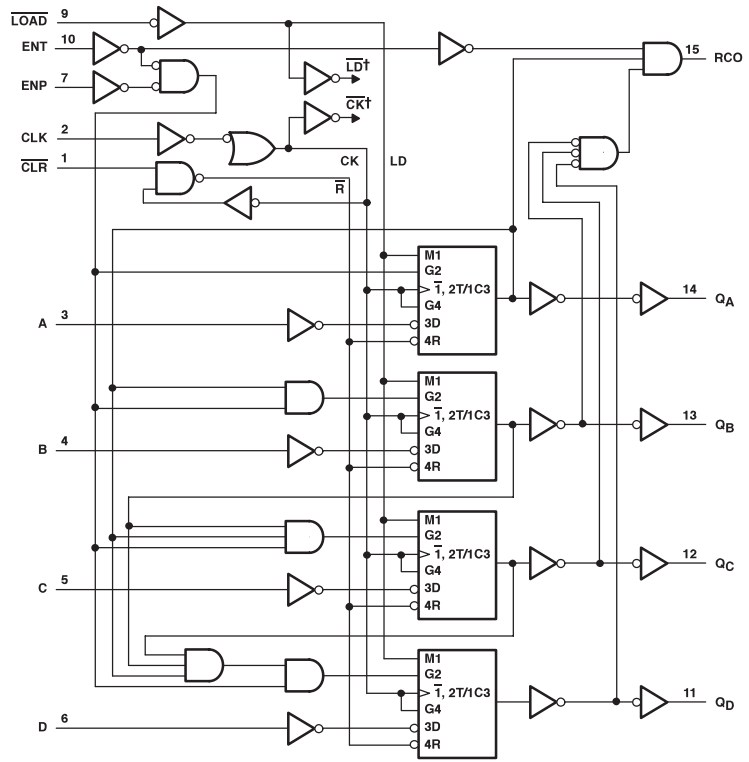
UNIT fmax : MHz, other : ns

163

SYNCHRONOUS 4-BIT BINARY COUNTERS

- Synchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	101	32	160	21	53	55	0.08	0.16	0.16	0.08	0.08	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	20	8	20	20	-4	4	4	24	24	-6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC
fmax				MIN	25	25	40	40	75	90	25
tw	CLOCK			MIN	25	25	10	-	-	7	20
	CLEAR				20	20	10	12.5	6.7	-	-
tsu	INPUT A, B, C, D			MIN	20	20	4	15	8	5	38
	ENABLE, P, T				20	20	12	15	8	11.5	43
	$\overline{LOAD}$				25	20	14	15	8	11.5	34
	$\overline{CLEAR}$				20	20	14	15	12	-	40
th				MIN	0	3	3	0	0	2	0
t_{PLH}		CLOCK	RIPPLE CARRY	MAX	35	35	25	20	16.5	15	54
t_{PHL}					35	35	25	20	12.5	15	54
t_{PLH}		CLOCK	ANY Q	MAX	25	24	15	15	7	9.5	51
t_{PHL}					29	27	15	20	13	11	51
t_{PLH}		ENABLE T	RIPPLE CARRY	MAX	16	14	15	13	9	8.5	49
t_{PHL}					16	14	15	13	8.5	8.5	49

PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax				MIN	20	20	103	91	50	85
tw	CLOCK			MIN	24	24	4.8	5.4	5	5
	CLEAR				-	-	-	-	-	-
tsu	INPUT A, B, C, D			MIN	18	15	4.4	4.4	6.5	4.5
	ENABLE, P, T				15	20	4.4	5.3	9	6
	$\overline{LOAD}$				18	18	5.3	6.6	9.5	6
	$\overline{CLEAR}$				20	20	5.3	6.6	4	3.5
th				MIN	3	5	0	0	1	1
t_{PLH}		CLOCK	RIPPLE CARRY	MAX	56	63	15.2	15.2	23.5	14
t_{PHL}					56	63	15.2	15.2	23.5	14
t_{PLH}		CLOCK	ANY Q	MAX	56	59	15	15	18.5	11.5
t_{PHL}					56	59	15	15	18.5	11.5
t_{PLH}		ENABLE T	RIPPLE CARRY	MAX	36	48	9.4	9.8	18	11.5
t_{PHL}					36	48	9.4	9.8	18	11.5

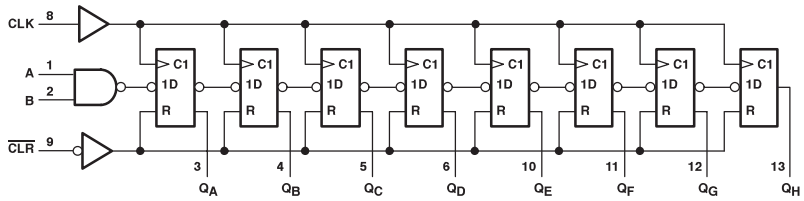
UNIT fmax : MHz, other : ns

164

8-BIT PARALLEL OUT SERIAL SHIFT REGISTERS

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS			
$\overline{CLEAR}$	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	54	27	24	0.08	0.16	0.16	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.4	-0.4	-0.4	-4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	8	8	8	4	4	4	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax				MIN	25	25	50	25	20	18	75	70
tw	$\overline{CLR}$ "L"			MIN	20	20	16	25	18	27	4.5	4.5
	CLK "H"			MIN	20	20	10	20	24	27	6.7	7.1
	CLK "L"			MIN	20	20	10	20	24	27	6.7	7.1
tsu	DATA			MIN	15	15	6	25	18	18	2.5	2.5
	$\overline{CLEAR}$ INACTIVE			MIN	20	20	8	25	18	18	2.5	2.5
th				MIN	5	5	2	5	4	4	2.5	3
t_{PHL}		$\overline{CLEAR}$	Q	MAX	42	36	20	51	42	57	13.9	15.8
t_{PLH}		CLOCK	Q	MAX	30	27	16	44	51	54	12.5	14.9
t_{PHL}					37	32	17	44	51	54	12.5	14.9

PARAMETER		INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
fmax				MIN	45	75
tw	$\overline{CLR}$ "L"			MIN	5	5
	CLK "H"			MIN	5	5
	CLK "L"			MIN	5	5
tsu	DATA			MIN	6	4.5
	$\overline{CLEAR}$ INACTIVE			MIN	2.5	2.5
th				MIN	0	1
t_{PHL}		$\overline{CLEAR}$	Q	MAX	18.5	12.5
t_{PLH}		CLOCK	Q	MAX	18.5	12.5
t_{PHL}					18.5	12.5

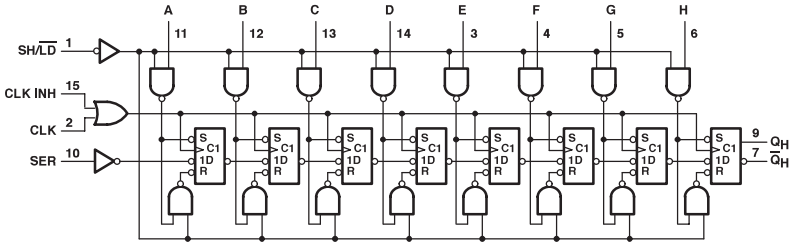
UNIT fmax : MHz, other : ns

165

8-BIT SHIFT REGISTERS

- Complementary Outputs: Serial (QH, $\overline{Q}$H)
- Direct Overriding Load (Data) Inputs
- Parallel-to-Serial Data Conversion

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ $\overline{LOAD}$	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	63	30	24	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	16	8	8	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax				MIN	20	25	45	25	20	18	50	85
tw	CLOCK	High		MIN	25	15	11	20	24	27	7	4
		Low		MIN	25	25	11	20	24	27	7	4
	SH/ $\overline{LD}$ "L"	High		MIN	15	25	-	-	-	-	-	-
		Low		MIN	15	17	12	20	24	30	9	6
tsu	CLK INH			MIN	30	30	11	25	24	30	5	3.5
	DATA				10	10	10	25	24	30	8.5	5
	SER				20	20	10	10	24	30	6	4
	SH/ $\overline{LD}$ "H"				45	45	10	20	-	-	6	4
th				MIN	0	0	4	5	11	11	0.5	1
t_{PLH}		CLOCK	Q_H or $\overline{Q}_H$	MAX	24	25	13	38	50	60	21.5	13.5
t_{PHL}					31	25	14	38	50	60	21.5	13.5
t_{PLH}		SH/ $\overline{LD}$	Q_H or $\overline{Q}_H$	MAX	31	35	20	38	53	60	22	13.5
t_{PHL}					40	35	22	38	53	60	22	13.5
t_{PLH}		H	Q_H	MAX	17	25	13	38	45	53	20	12.5
t_{PHL}					36	30	16	38	45	53	20	12.5
t_{PLH}		H	$\overline{Q}_H$	MAX	27	30	15	38	45	53	20	12.5
t_{PHL}					27	25	16	38	45	53	20	12.5

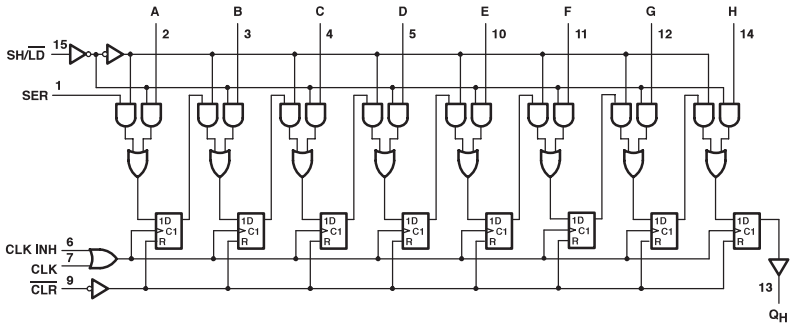
UNIT fmax : MHz, other : ns

166

8-BIT SHIFT REGISTERS

- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	127	32	24	60	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-1	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	16	8	8	20	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax				MIN	25	25	45	110	25	20	16	50	85
tw	CLOCK			MIN	20	20	10	3.5	20	24	30	7	4
	$\overline{CLEAR}$				20	25	9	4	25	30	53	7	5
tsu	Mode Control			MIN	30	30	16	4	36	44	45	6	4
	DATA				20	20	7	3	20	24	24	6	4.5
th				MIN	0	0	3	0	0	1	0	0	1
t_{PHL}		$\overline{CLEAR}$	QH	MAX	35	30	14	9.5	30	48	60	18.5	12
t_{PHL}		CLOCK	QH	MAX	30	25	13	14	38	48	60	21.5	13.5
t_{PLH}					26	20	12	9	38	48	60	21.5	13.5

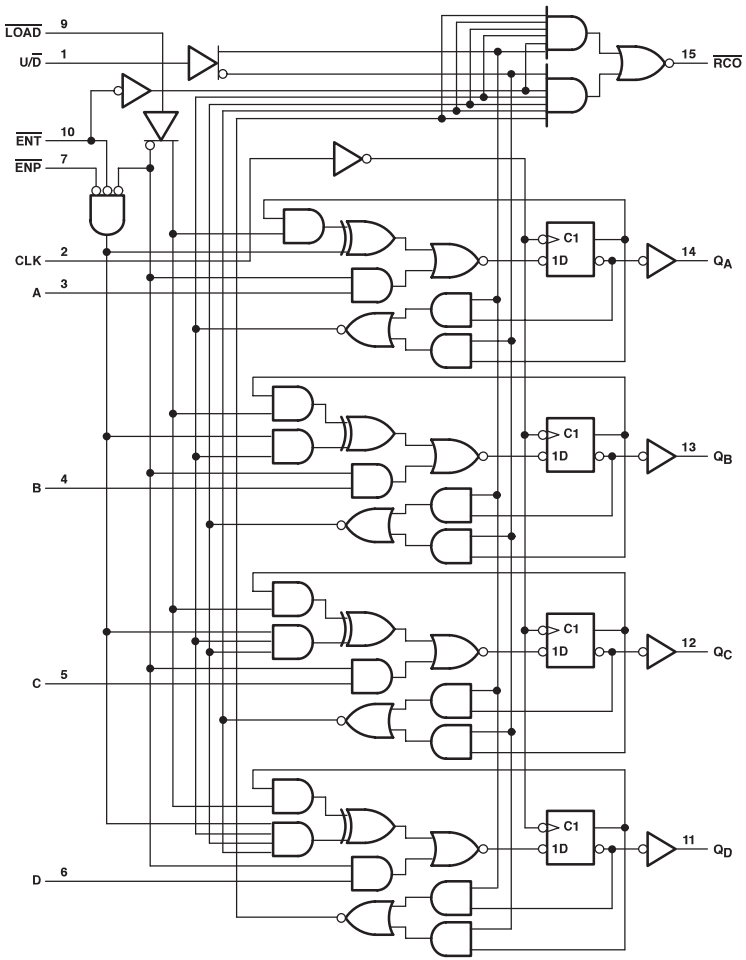
UNIT fmax : MHz, other : ns

169

4-BIT UP/DOWN SYNCHRONOUS ONOUS BINARY COUNTERS

- Fully Synchronous Operation for Counting and Programming
- Internal Carry Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	S	ALS	AS	F	UNIT
I_{CC}		MAX	45	160	25	63	52	mA
I_{OH}	$\overline{RCO}$	MAX	-0.4	-1	-0.4	-2	-1	mA
	Q	MAX	-1.2	-1	-0.4	-2	-1	mA
I_{OL}	$\overline{RCO}$	MAX	8	20	8	20	20	mA
	Q	MAX	24	20	8	20	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F
fmax			MIN	20	40	40	75	90
t_{PLH}	CLK	$\overline{RCO}$	MAX	40	21	20	16.5	17
t_{PHL}				25	28	20	13	12.5
t_{PLH}	CLK	ANY Q	MAX	25	15	15	13	9.5
t_{PHL}				25	15	20	7	13
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	MAX	25	12	13	9	7
t_{PHL}				20	25	16	9	9
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	MAX	35	15	19	12	12.5
t_{PHL}				25	22	19	13	12

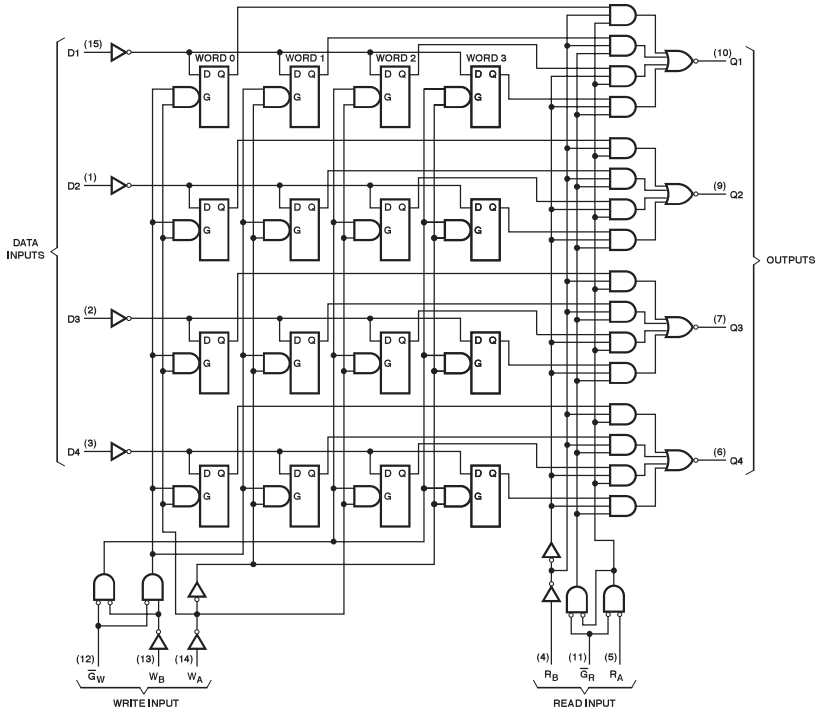
UNIT fmax : MHz, other : ns

170

4-BY-4 REGISTER FILES

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times: Typically 20ns
- Expandable to 1024 Words of 4 Bits

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

WRITE FUNCTION TABLE

WRITE INPUTS			OUTPUTS			
W_B	W_A	$\overline{G}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
R_B	R_A	$\overline{G}_R$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	150	40	mA
V_{OH}	MAX	5.5	5.5	V
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax				MIN		
tw				MIN	25	25
tsu	D			MIN	10	10
	W				15	15
th	D			MIN	15	15
	W				5	5
t_{PLH}		READ ENABLE	Q	MAX	15	30
t_{PHL}					30	30
t_{PLH}		READ SELECT	Q	MAX	35	40
t_{PHL}					40	40
t_{PLH}		WRITE ENABLE	Q	MAX	40	45
t_{PHL}					45	40
t_{PLH}		DATA	Q	MAX	30	45
t_{PHL}					45	35

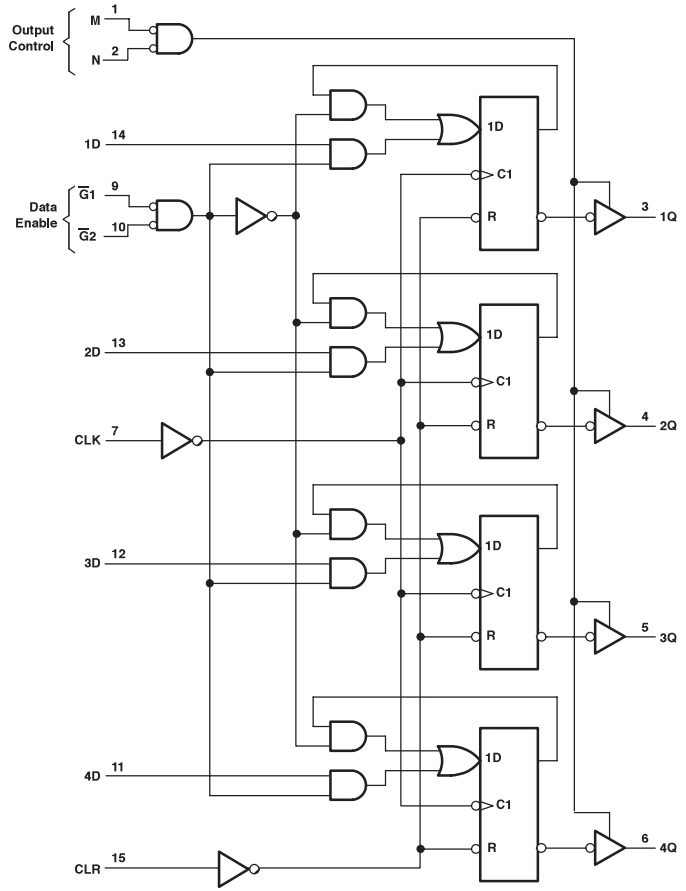
UNIT fmax : MHz, other : ns

173

4-BIT D-TYPE REGISTERS

- 3-State Outputs Interface Directly
- Fully Independent Clock Virtually

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
CLEAR	CLOCK	DATA $\overline{G1}$	ENABLE $\overline{G2}$	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_O
L	↑	H	X	X	Q_O
L	↑	X	H	X	Q_O
L	↑	L	L	L	L
L	↑	L	L	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	72	24	0.08	0.16	0.16	mA
I_{OH}	MAX	-5.2	-2.6	-6	-6	-6	mA
I_{OL}	MAX	16	24	6	6	6	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	25	20	13
t_W				MIN	20	25	20	24	28
t_{su}	DATA ENABLE			MIN	17	35	25	18	18
	DATA				10	17	25	18	27
	CLR INACTIVE			MIN	10	10	23	-	-
t_h	DATA ENABLE			MIN	2	0	0	0	0
	DATA				10	3	0	3	0
t_{PHL}		CLEAR	Q	MAX	27	35	38	53	66
t_{PLH}		CLOCK	Q	MAX	43	25	38	60	60
t_{PHL}					31	30	38	60	60
t_{PZH}		ENABLE	Q	MAX	30	23	38	45	45
t_{PZL}					30	27	38	45	45
t_{PHZ}		DISABLE	Q	MAX	14	20	38	45	-
t_{PLZ}					20	17	38	45	-

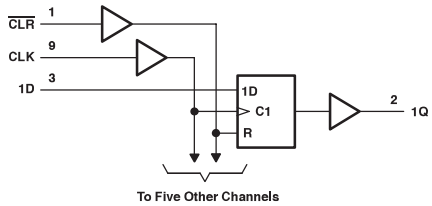
UNIT fmax : MHz, other : ns

174

HEX D-TYPE FLIP-FLOPS

- Buffered Clock and Direct Clear Inputs
- Fully Buffered Outputs for Maximum Isolation from External Disturbances

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{CLEAR}$	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
L	L	X	Q_O

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	65	26	144	19	45	55	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-24	-24	-8	-8	-6	-12	mA
I_{OL}	MAX	24	24	8	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC
fmax				MIN	25	30	75	50	100	80	25	20	17	95
t_W	$\overline{CLR}$ LOW			MIN	20	20	10	10	5	5	20	24	38	4
	CLK HIGH			MIN	20	20	7	10	4	4	20	24	30	5.2
	CLK LOW				20	20	7	10	6	6	20	24	30	5.2
t_{su}	DATA INPUT			MIN	20	20	5	10	4	4.5	25	18	24	2
	$\overline{CLR}$ INACTIVE			MIN	25	25	5	6	6	5	25	-	-	-
t_h				MIN	5	5	3	0	1	1	0	5	5	3
t_{PLH}		$\overline{CLR}$	ANY Q	MAX	25	-	-	18	-	-	40	45	66	14.5
t_{PHL}					35	35	22	23	14	15	40	45	66	14.5
t_{PLH}		CLK	ANY Q	MAX	30	30	12	15	8	9	40	50	60	13.5
t_{PHL}					35	30	17	17	10	11	40	50	60	13.5

PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
fmax				MIN	80	80	65	50	80
t_W	$\overline{CLR}$ LOW			MIN	4	5	5	5	5
	CLK HIGH			MIN	6.2	5	5	5	5
	CLK LOW				6.2	5	5	5	5
t_{su}	DATA INPUT			MIN	2	4.5	5	6	4.5
	$\overline{CLR}$ INACTIVE			MIN	-	2.5	3.5	3	2.5
t_h				MIN	2.5	0.5	0	0	0.5
t_{PLH}		$\overline{CLR}$	ANY Q	MAX	15.5	-	-	17	11
t_{PHL}					15.5	11	13	17	11
t_{PLH}		CLK	ANY Q	MAX	14	10.5	10	16.5	10.5
t_{PHL}					14	10.5	10	16.5	10.5

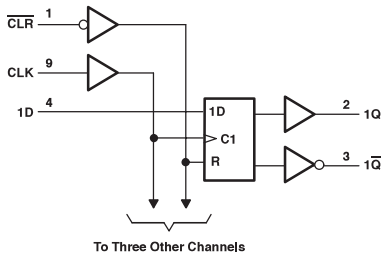
UNIT fmax : MHz, other : ns

175

QUAD D-TYPE FLIP-FLOPS

- Complementary Outputs (Q, $\overline{Q}$)
- Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	45	18	96	14	34	34	0.04	0.16	0.16	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	24	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	30	75	50	100	100	25	20	16
tw	$\overline{CLR}$ LOW			MIN	20	20	10	10	5	5	20	24	30
	CLK HIGH				20	20	7	10	4	4	20	24	30
	CLK LOW				20	20	7	10	5	5	20	24	30
tsu	DATA INPUT			MIN	20	20	5	10	3	3	25	24	30
	$\overline{CLR}$ INACTIVE				25	25	5	6	6	5	25	-	-
th				MIN	5	5	3	0	1	1	0	5	5
t_{PLH}		$\overline{CLR}$	ANY Q or $\overline{Q}$	MAX	25	30	15	18	9	9	38	53	53
t_{PHL}					35	30	22	23	13	13	38	53	53
t_{PLH}		CLK	ANY Q or $\overline{Q}$	MAX	30	25	12	15	7.5	7.5	38	53	50
t_{PHL}					35	25	17	17	10	9.5	38	53	50

PARAMETER		INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax				MIN	125	100	114	45	75
tw	$\overline{CLR}$ LOW			MIN	4	4	4	5	5
	CLK HIGH				4	5	5	5	5
	CLK LOW				4	5	5	5	5
tsu	DATA INPUT			MIN	5.5	2	2	5	4
	$\overline{CLR}$ INACTIVE				5.5	-	-	5	5
th				MIN	0.5	2	2	1	1
t_{PLH}		$\overline{CLR}$	ANY Q or $\overline{Q}$	MAX	6.8	12.2	13	15.5	9.5
t_{PHL}					9.3	12.2	13	15.5	9.5
t_{PLH}		CLK	ANY Q or $\overline{Q}$	MAX	6.9	12.2	11.5	17	10.5
t_{PHL}					9..3	12.2	11.5	17	10.5

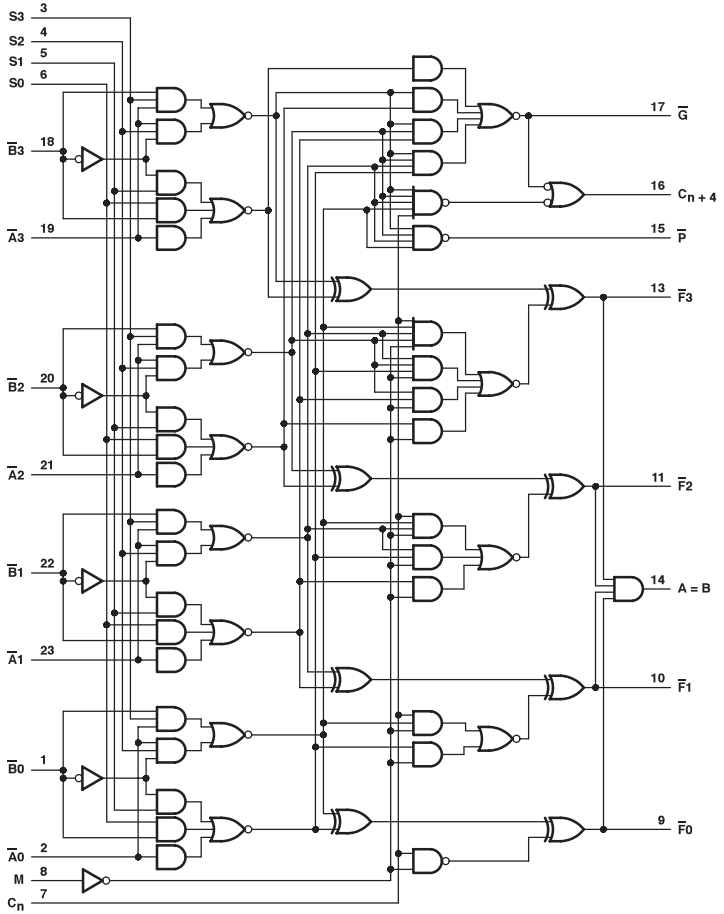
UNIT fmax : MHz, other : ns

181

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects

Logic Diagram



FUNCTION TABLE (ACTIVE LOW)

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTION	Cn = L (no carry)	Cn = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{A+B}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A}+B$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1(2's COMP)	F = 0
L	H	L	L	$F = \overline{A+B}$	F = A PLUS $(A+\overline{B})$	F = A PLUS $(A+\overline{B})$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS $(A+\overline{B})$	F = AB PLUS $(A+\overline{B})$ PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A+\overline{B}$	$F = A+\overline{B}$	F = $(A+\overline{B})$ PLUS 1
H	L	L	L	$F = \overline{AB}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = A\overline{B}$ PLUS (A + B)	$F = A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = $(A+\overline{B})$	F = $(A+\overline{B})$ PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	$F = A\overline{B}$	$F = A\overline{B}$ PLUS A	$F = A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A PLUS 1	F = A PLUS 1

FUNCTION TABLE (ACTIVE HIGH)

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTION	$\overline{C}n$ = H (no carry)	$\overline{C}n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{AB}$	$F = A+\overline{B}$	F = $(A+\overline{B})$ PLUS 1
L	L	H	H	F = 0	F = MINUS 1(2's COMPL)	F = 0
L	H	L	L	$F = \overline{AB}$	F = A PLUS $A\overline{B}$	F = A PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS $A\overline{B}$	F = (A + B) PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A}+B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A+\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

RECOMMENDED OPERATING CONDITIONS

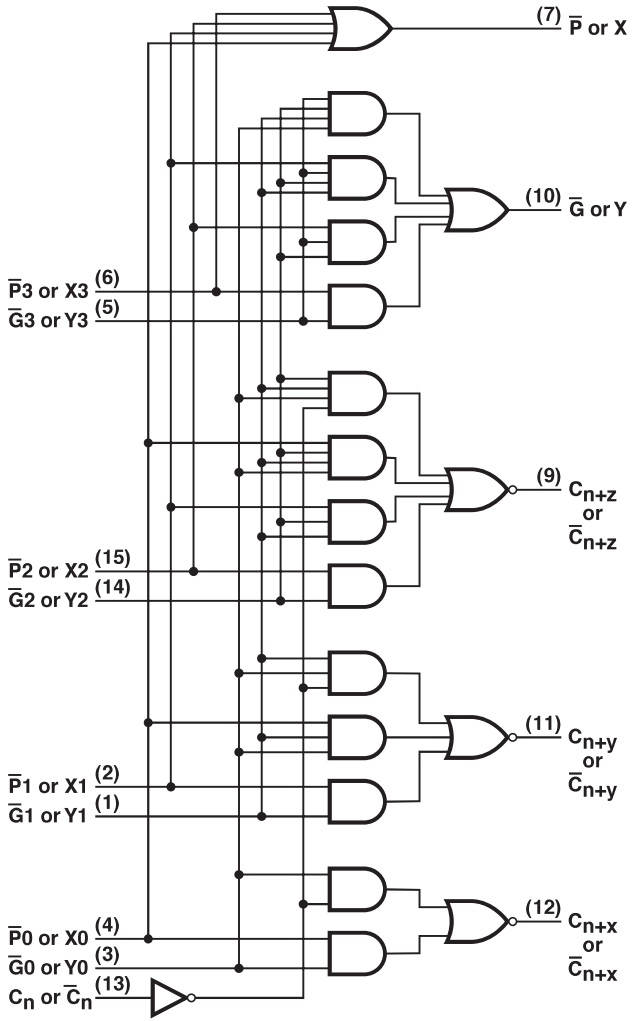
PARAMETER		MAX or MIN	TTL	LS	S	AS	UNIT
I_{CC}		MAX	150	37	220	200	mA
I_{OH}	All outputs except $\overline{A} = B$	MAX	-0.8	-0.4	-1	-2	mA
	$\overline{G}$		-	-	-	-3	mA
I_{OL}	All outputs except $\overline{G}$	MAX	16	8	20	20	mA
	$\overline{G}$		16	8	20	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS
t_{PLH}	C_n	C_{n+4}	MAX	18	27	10.5	9
t_{PHL}				19	20	10.5	9
t_{PLH}	$\overline{A}$, $\overline{B}$	C_{n+4}	MAX	43	38	18.5	12
t_{PHL}				41	38	18.5	12
t_{PLH}	C_n	$\overline{F}$	MAX	19	26	12	9
t_{PHL}				18	20	12	9
t_{PLH}	$\overline{A_i}$, $\overline{B_i}$	$\overline{F_i}$	MAX	42	32	16.5	9.5
t_{PHL}				32	20	16.5	8

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

$\overline{G}$ OUTPUTS

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

$\overline{P}$ OUTPUTS

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

C_{n+x} OUTPUTS

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

C_{n+y} OUTPUTS

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

C_{n+z} OUTPUTS

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	S	AS	UNIT
I_{CC}	MAX	72	109	36	mA
I_{OH}	MAX	-0.8	-1	-2	mA
I_{OL}	MAX	16	20	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	S	AS
t_{PLH}	Cn	Cn + X, Cn + Y or Cn + Z	MAX	10	10	10
t_{PHL}				10.5	10.5	9.5
t_{PLH}	P or $\overline{G}$	Cn + X, Cn + Y or Cn + Z	MAX	7	7	10.5
t_{PHL}				7	7	6
t_{PLH}	P or $\overline{G}$	$\overline{G}$	MAX	7.5	7.5	12
t_{PHL}				10.5	10.5	8
t_{PLH}	$\overline{P}$	$\overline{P}$	MAX	6.5	6.5	7.5
t_{PHL}				10	10	6

UNIT: ns

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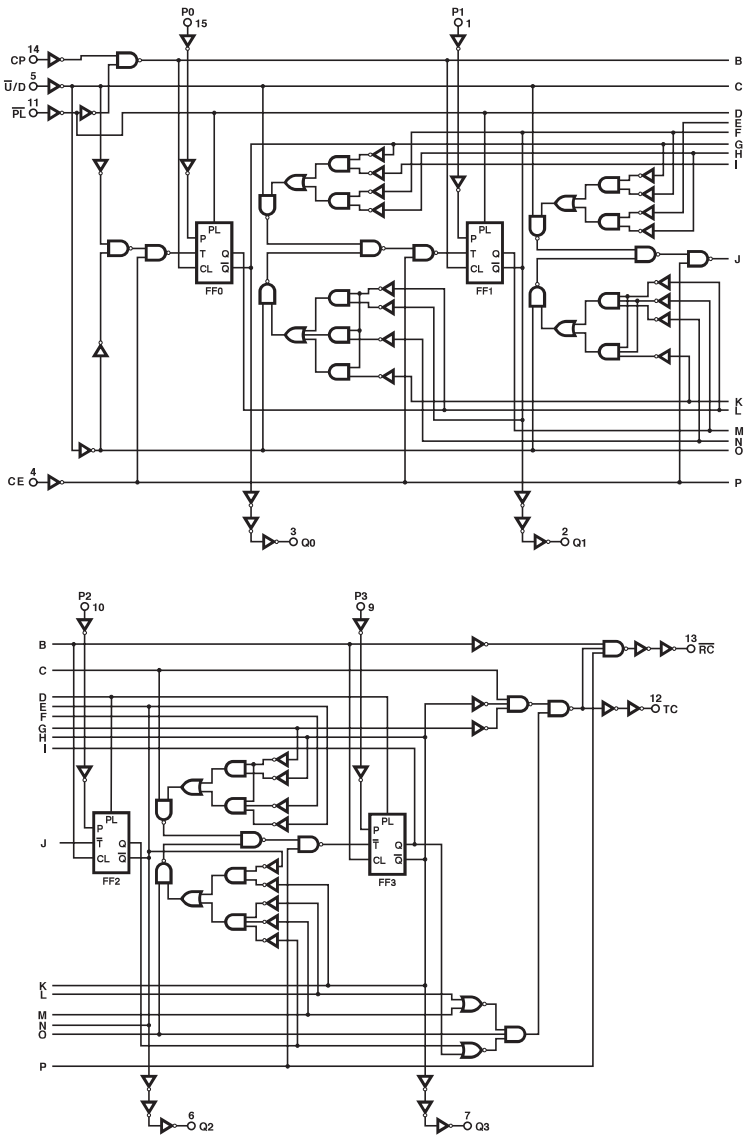
SYNCHRONOUS UP/DOWN DECADE COUNTER

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	105	35	22	0.08	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-4	-4	mA
I_{OL}	MAX	16	8	8	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC
fmax			MIN	20	20	25	17	25
tw	CLK (CP)		MIN	25	25	20	30	20
	$\overline{LOAD}$ ($\overline{PL}$)			35	35	20	30	25
tsu	Data , high or low		MIN	20	20	20	38	15
th	Data hold time		MIN	0	5	5	5	2
t_{PLH}	$\overline{LOAD}$ (PL)	Q	MAX	33	33	30	66	49
t_{PHL}				50	50	30	66	49
t_{PLH}	DATA	Q	MAX	22	32	21	60	44
t_{PHL}				50	40	21	60	44
t_{PLH}	CLK (CP)	$\overline{RCO}$ ($\overline{RC}$)	MAX	20	20	20	30	31
t_{PHL}				24	24	20	30	31
t_{PLH}	CLK (CP)	Q	MAX	24	24	18	48	43
t_{PHL}				36	36	18	48	43
t_{PLH}	CLK (CP)	MAX/MIN (TC)	MAX	42	42	31	63	53
t_{PHL}				52	52	31	63	53
t_{PLH}	D/$\overline{U}$ (U/D)	$\overline{RCO}$ ($\overline{RC}$)	MAX	45	45	37	57	38
t_{PHL}				45	45	28	57	38
t_{PLH}	D/$\overline{U}$ (U/D)	MAX/ MIN (TC)	MAX	33	33	25	48	41
t_{PHL}				33	33	25	48	41

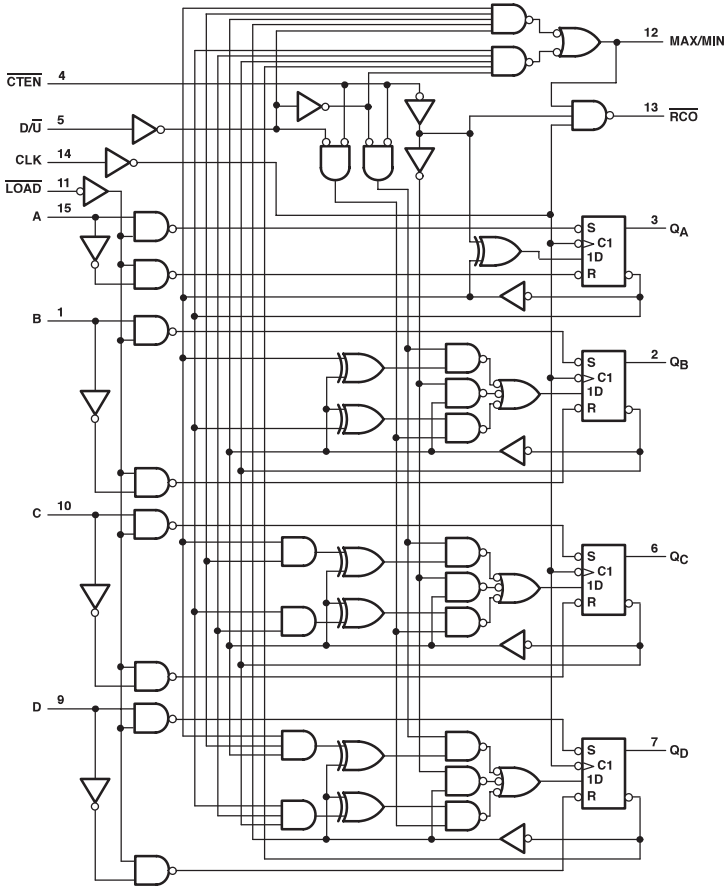
UNIT fmax : MHz other : ns

191

SYNCHRONOUS UP/DOWN COUNTERS

- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presentable with Load Control

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	105	35	22	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	8	4	4	4	mA

SWITCHING CHARACTERISTICS

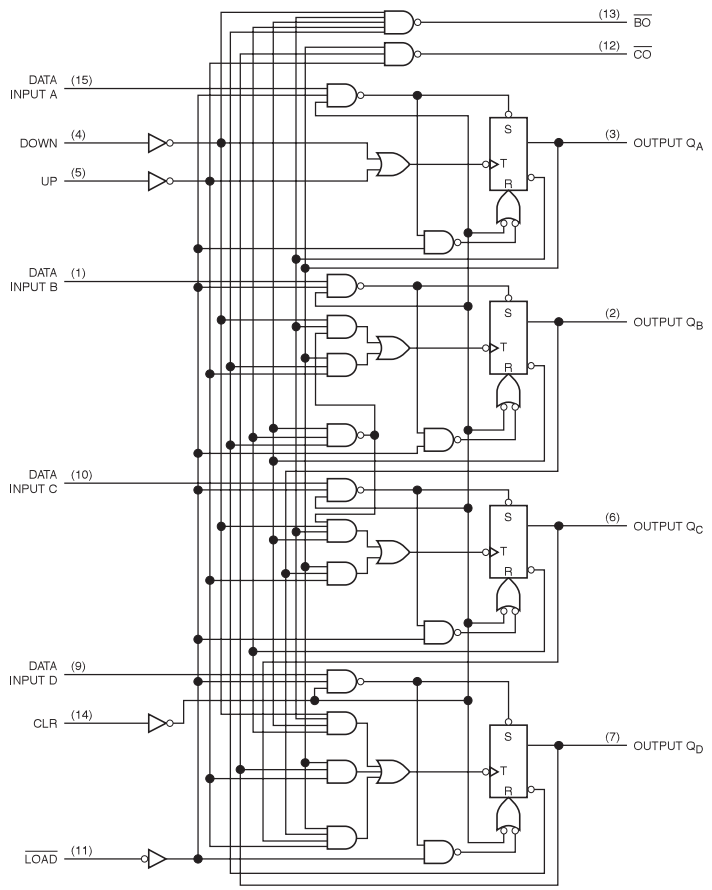
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	20	20	30	17	25	25
tw	CLK			MIN	25	25	16.5	30	20	20
	LOAD				35	35	20	30	25	25
tsu	DATA			MIN	20	20	20	38	15	15
th	DATA			MIN	0	5	5	5	2	2
t_{PLH}		$\overline{LOAD}$	QA, QB QC, QD	MAX	33	33	30	66	49	50
t_{PHL}					50	50	30	66	49	50
t_{PLH}		DATA A, B, C, D	QA, QB QC, QD	MAX	22	32	21	60	44	48
t_{PHL}					50	40	21	60	44	48
t_{PLH}		CLK	RIPPLE CLK	MAX	20	20	20	30	31	34
t_{PHL}					24	24	20	30	31	34
t_{PLH}		CLK	QA, QB QC, QD	MAX	24	24	18	48	43	44
t_{PHL}					36	36	18	48	43	44
t_{PLH}		CLK	MAX or MIN	MAX	42	42	31	63	53	53
t_{PHL}					52	52	31	63	53	53
t_{PLH}		D/$\overline{U}$	RIPPLE CLK	MAX	45	45	37	57	38	38
t_{PHL}					45	45	28	57	38	38
t_{PLH}		D/$\overline{U}$	MAX or MIN	MAX	33	33	25	48	41	48
t_{PHL}					33	33	25	48	41	48

UNIT fmax : MHz, other : ns

192

PRESETTABLE SYNCHRONOUS 4-BITUP/DOWN COUNTERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FANCTION
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset inputs

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_w	CPU, CPD		MIN	35
	$\overline{PL}$			24
	MR			30
t_{su}	Pn to $\overline{PL}$		MIN	24
t_h	Pn to $\overline{PL}$		MIN	0
	CPD to CPU, CPD to CPU			24
t_{PLH}	CPU	$\overline{TCU}$	MAX	38
t_{PHL}				38
t_{PLH}	CPD	$\overline{TCD}$	MAX	38
t_{PHL}				38
t_{PLH}	CPD	Qn	MAX	65
t_{PHL}				65
t_{PLH}	CPD	Qn	MAX	65
t_{PHL}				65
t_{PLH}	$\overline{PL}$	Qn	MAX	66
t_{PHL}				66
t_{PHL}	MR	Qn	MAX	60

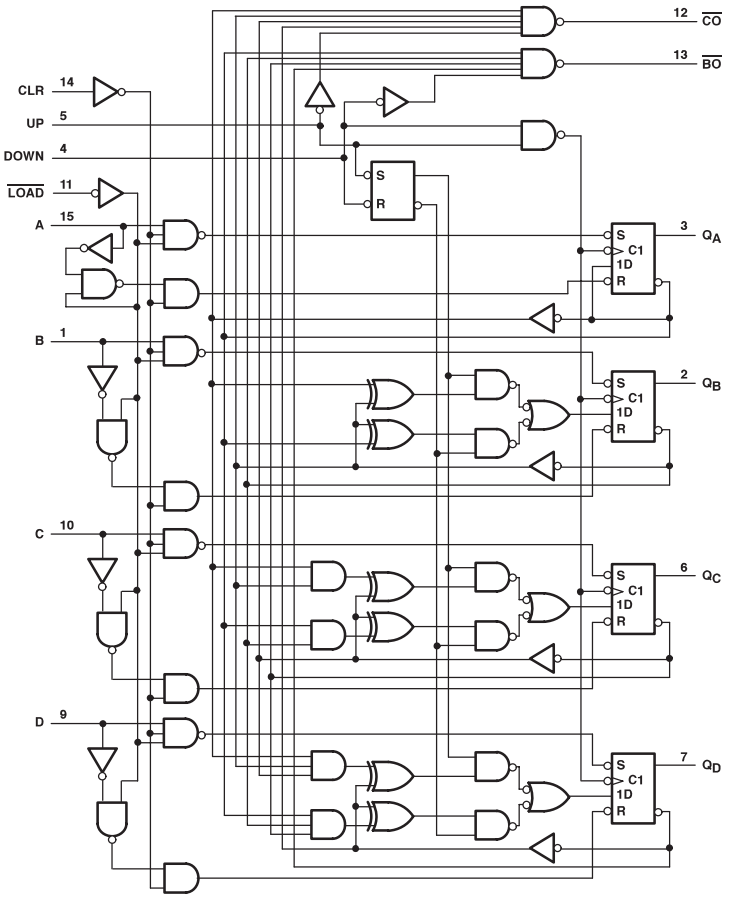
UNIT:ns

193

SYNCHRONOUS UP/DOWN DUAL CLOCKCOUNTERS

- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	102	34	22	54	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.4	-0.4	-0.4	-1	-4	-4	-4	mA
I_{OL}	MAX	16	8	8	20	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	30	85	17	17	15
tw				MIN	20	20	20	4	30	30	35
tsu	DATA			MIN	20	20	20	3.5	28	24	22
th	DATA			MIN	0	5	5	2.5	5	0	0
t_{PLH}		UP	$\overline{CO}$	MAX	26	26	16	9	41	38	41
t_{PHL}					24	24	18	9	41	38	41
t_{PLH}		DOWN	$\overline{BO}$	MAX	24	24	16	9	41	38	41
t_{PHL}					24	24	18	9	41	38	41
t_{PLH}		UP or DOWN	ANY Q	MAX	38	38	19	9	63	65	60
t_{PHL}					47	47	17	13	63	65	60
t_{PLH}		$\overline{LOAD}$	ANY Q	MAX	40	40	30	11	65	66	69
t_{PHL}					40	40	28	13	65	66	69
t_{PHL}		CLR	ANY Q	MAX	35	35	17	12	60	60	65

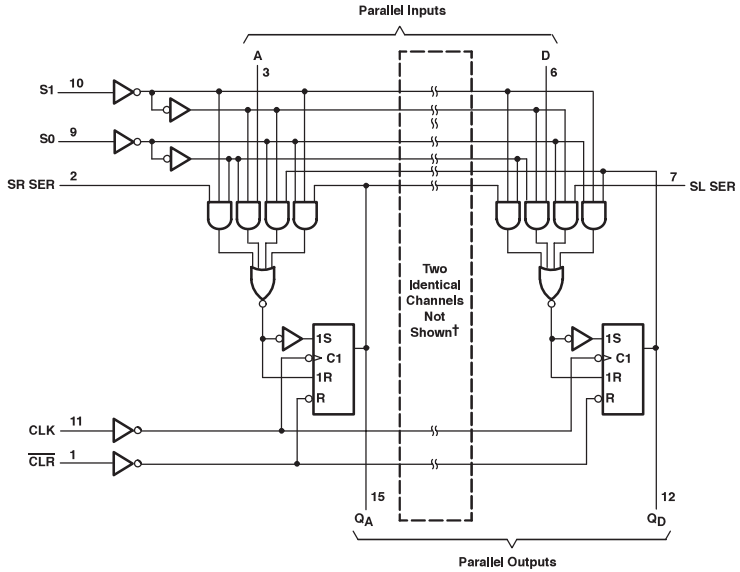
UNIT fmax : MHz, other : ns

194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts

Logic Diagram



† I/O ports not shown: Q_B (14) and Q_C (13)

FUNCTION TABLE

INPUTS									OUTPUTS			
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL						
	S1	S0		LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	63	23	135	53	0.1	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2	-4	-4	-4	mA
I_{OL}	MAX	16	8	20	20	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	70	80	25	20	18
tw	$\overline{CLR}$			MIN	20	20	12	4.5	20	24	24
	CLK "H"				20	20	7	4	20	24	24
	CLK "H"				20	20	7	7	20	24	24
tsu	Mode Control			MIN	30	30	11	9.5	25	24	30
	DATA				20	20	5	4	25	21	21
	CLR INACTIVE				25	25	9	6	-	-	-
th				MIN	0	0	3	0.5	0	0	0
t_{PHL}		$\overline{CLEAR}$	ANY	MAX	30	30	18.5	12	38	42	60
t_{PLH}		CLOCK	ANY	MAX	22	22	12	7	36	53	56
t_{PHL}					26	26	16.5	7	36	53	56

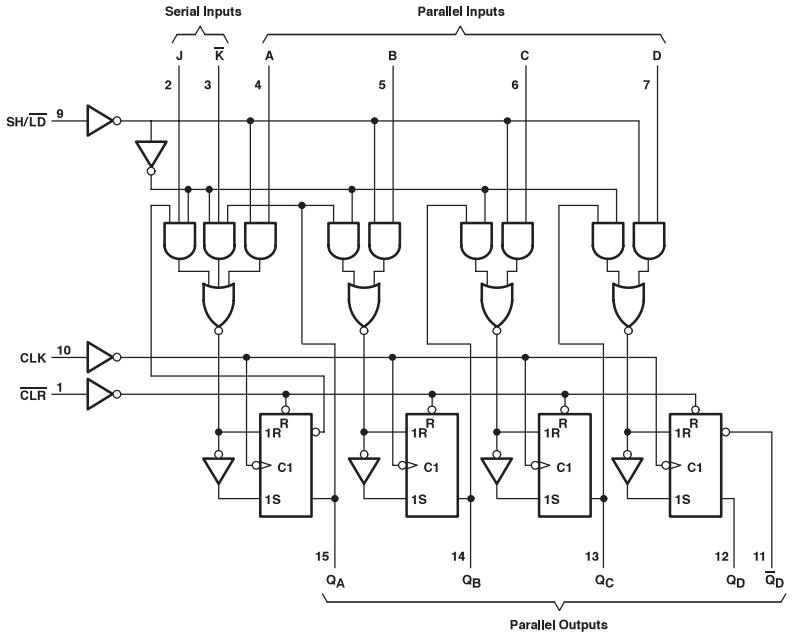
UNIT fmax : MHz, other : ns

195

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions

Logic Diagram



FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	63	21	109	57	0.1	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2	-4	-4	mA
I_{OL}	MAX	16	8	20	20	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC
fmax				MIN	30	30	70	70	25	20
tw	CLOCK			MIN	16	16	7	4	20	24
	$\overline{CLEAR}$				12	12	12	7.2	20	24
tsu	Shift / Load			MIN	25	25	11	8	25	30
	Serial & Pararel Data				20	15	5	3.5	25	30
	Clear Inactive Data				25	25	9	6	25	30
TRELEASE				MAX	10	20	6	-	-	-
th				MIN	0	0	3	1	0	-
t_{PHL}		$\overline{CLEAR}$	QA, QD	MAX	30	30	18.5	11.5	38	45
t_{PLH}		CLOCK		MAX	22	22	12	8.5	36	53
t_{PHL}					26	26	16.5	10.5	36	53

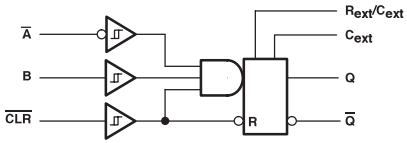
UNIT fmax : MHz, other : ns

221

DUAL MONOSTABLE MULTIVIBRATORS

- Overriding Clear Terminates Outputs Pulse

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍	⎏
H	↓	H	⎍	⎏
↑	L	H	⎍	⎏

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	80	27	0.16	0.16	0.28	0.65	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-6	-12	mA
I_{OL}	MAX	16	8	4	4	6	12	mA

SWITCHING CHARACTERISTICS

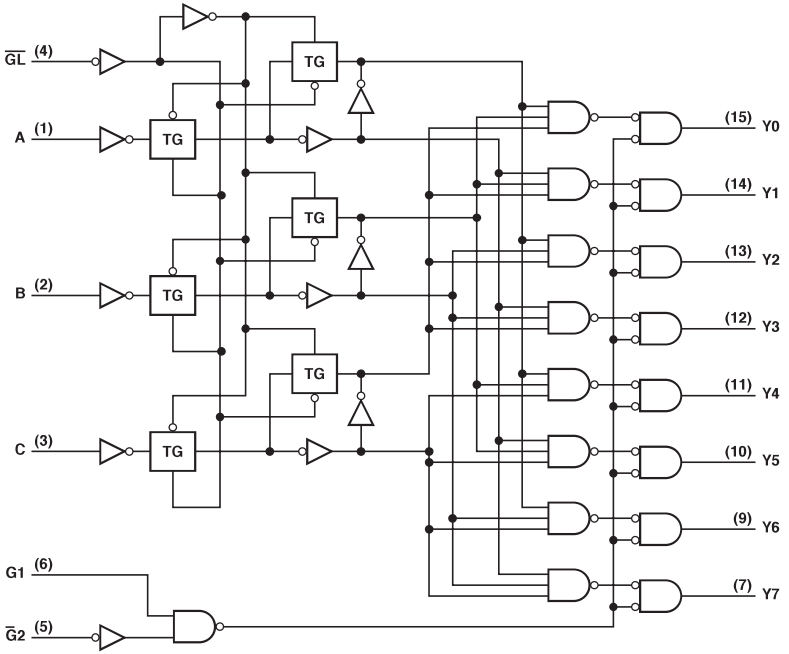
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	A (HC, LV: $\overline{A}$)	Q	MAX	70	70	63	63	27.5	16
	B			55	55	63	63	27.5	16
t_{PHL}	A (HC, LV: $\overline{A}$)	$\overline{Q}$	MAX	80	80	51	51	27.5	16
	B			65	65	51	51	27.5	16
t_{PHL}	Clear	Q	MAX	27	55	48	57	22	13
t_{PLH}		$\overline{Q}$		40	65	54	56	22	13

UNIT: ns

237

3-TO-8 LINE DECODER DEMULTIPLEXER WITH ADDRESS LATCHES

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS							
LE	OE0	$\overline{OE1}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

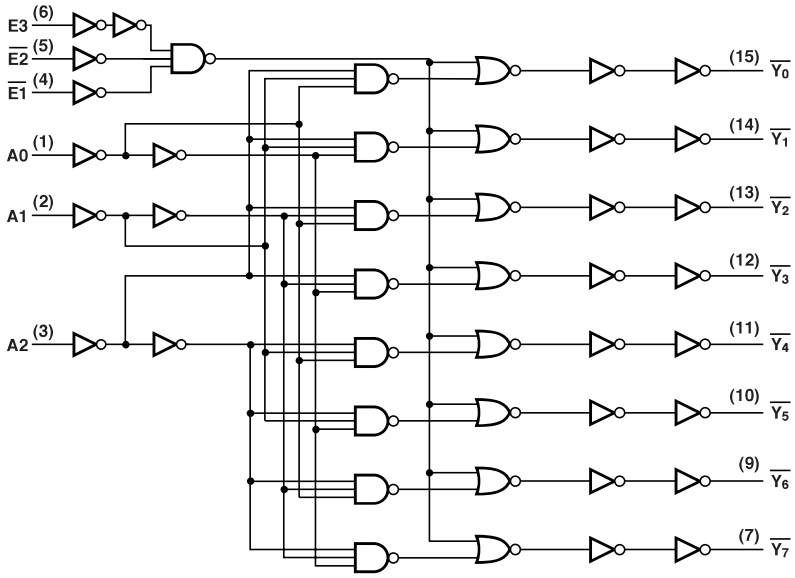
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_w	LE Pulse Width		MIN	20	15	15
t_{su}	An to LE		MIN	19	15	15
t_h	An to LE		MIN	5	9	5
t_{PLH}	An	Y	MAX	48	48	57
t_{PHL}				48	48	57
t_{PLH}	OE	Y	MAX	44	44	60
t_{PHL}				44	44	60

UNIT:ns

3-TO-8-LINE DECODERS/DEMULTIPLEXERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	$\overline{A0}$	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

Note: H = High Voltage Level, L = Low Volltage Level, X = Don't Care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-24	-24	mA
I_{OL}	MAX	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	Address	Y	MAX	45	53	15	15
t_{PHL}				45	53	15	15
t_{PLH}	$\overline{E1}$, $\overline{E2}$	Y	MAX	-	-	11.9	11.9
t_{PHL}				-	-	11.9	11.9
t_{PLH}	E3	Y	MAX	-	-	16.6	16.6
t_{PHL}				-	-	16.6	16.6

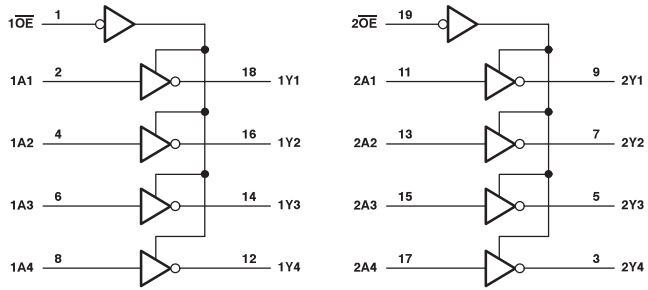
UNIT:ns

240

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V	UNIT
I_{CCH}	MAX	27	135	11	11	17	29	0.08	0.16	0.08	0.16	31	0.25	0.19	mA
I_{CCL}	MAX	44	150	23	23	75	75	0.08	0.16	0.08	0.16	71	30	5	mA
I_{CCZ}	MAX	50	150	25	25	38	63	0.08	0.16	0.08	0.16	9	0.25	0.19	mA
I_{OH}	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	mA
I_{OL}	MAX	24	64	24	48	64	64	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCZ 3V	UNIT
I_{CCH}	MAX	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.1	mA
I_{CCL}	MAX	5	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.1	mA
I_{CCZ}	MAX	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.1	mA
I_{OH}	MAX	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
I_{OL}	MAX	64	24	24	24	24	24	24	8	8	8	16	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V
t_{PLH}	A	Y	MAX	14	7	9	9	6.5	8	25	30	32	33	5.6	4.8	3.8
t_{PHL}				18	7	9	9	6.5	5.7	25	30	32	33	4	4.8	4
t_{PZH}	$\overline{G}$	Y	MAX	23	10	13	13	6.4	6.1	38	-	44	-	8.8	5.2	4.6
t_{PZL}				30	15	18	18	9	10	38	-	44	-	10.5	6.2	4.4
t_{PHZ}	$\overline{G}$	Y	MAX	25	9	10	10	5	6.3	38	-	44	-	8.1	6.4	4.4
t_{PLZ}				20	15	12	12	9.5	9.5	38	-	44	-	9.5	5.8	4.3

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCZ 3V
t_{PLH}	A	Y	MAX	3.8	8.4	7	7.2	10.6	9.5	8.6	8.5	9.5	12.5	8.5	6.5	6.5
t_{PHL}				4	7.2	6.5	7.2	8.7	8.5	8.6	8.5	9.5	12.5	8.5	6.5	6.5
t_{PZH}	$\overline{G}$	Y	MAX	4.6	9.2	8	12	12.5	9.5	13.4	10.5	13	16	10.5	8	8
t_{PZL}				4.4	8.7	8.5	12	12.3	10.5	13.4	10.5	13	16	10.5	8	8
t_{PHZ}	$\overline{G}$	Y	MAX	4.4	6.6	9.5	12	10	10.5	13.4	10.5	13	17	15.5	7	7
t_{PLZ}				4.3	7.7	9.5	12	10.8	10.5	13.4	10.5	13	17	15.5	7	7

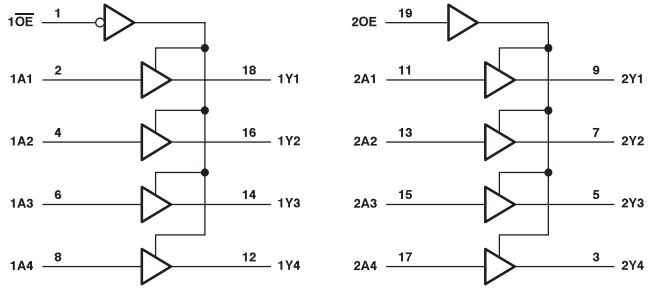
UNIT: ns

241

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	UNIT
I_{CCH}	MAX	27	160	18	35	60	0.08	0.16	0.16	43	0.25	0.19	0.04	mA
I_{CCL}	MAX	46	180	26	90	90	0.08	0.16	0.16	85	30	5	0.04	mA
I_{CCZ}	MAX	54	180	30	56	90	0.08	0.16	0.16	10	0.25	0.19	0.04	mA
I_{OH}	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-15	-32	-32	-24	mA
I_{OL}	MAX	24	64	24	64	64	6	6	6	64	64	64	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	UNIT
I_{CCH}	MAX	0.04	0.16	mA
I_{CCL}	MAX	0.04	0.16	mA
I_{CCZ}	MAX	0.04	0.16	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC
t_{PLH}	A	Y	MAX	18	9	11	6.2	6.2	29	33	38	4.9	4.6	3.5	7.5
t_{PHL}				18	9	10	6.2	6.5	29	33	38	5.9	4.6	3.4	7.5
t_{PZH}	$1\overline{G}$	Y	MAX	23	12	21	9	6.7	38	-	-	8.7	6.8	4.5	9.5
t_{PZL}				30	15	21	7.5	8	38	-	-	9.4	6.8	4.4	9.5
t_{PHZ}	$1\overline{G}$	Y	MAX	25	9	10	6	7	38	-	-	8.1	7.1	4.5	10.5
t_{PLZ}				20	15	15	9	7	38	-	-	9.9	5.9	4.7	10.5
t_{PZH}	2G	Y	MAX	23	12	21	10.5	6.7	38	-	-	8.7	6.8	4.5	9.5
t_{PZL}				30	15	21	8.5	8	38	-	-	9.4	6.8	4.4	9.5
t_{PHZ}	2G	Y	MAX	25	9	10	7	7	38	-	-	8.1	7.1	4.5	10.5
t_{PLZ}				20	15	15	12	7	38	-	-	9.9	5.9	4.7	10.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT
t_{PLH}	A	Y	MAX	9.5	9.6
t_{PHL}				8.5	9.6
t_{PZH}	$1\overline{G}$	Y	MAX	9.5	13.4
t_{PZL}				10.5	13.4
t_{PHZ}	$1\overline{G}$	Y	MAX	10.5	13.4
t_{PLZ}				10.5	13.4
t_{PZH}	2G	Y	MAX	9.5	13.4
t_{PZL}				10.5	13.4
t_{PHZ}	2G	Y	MAX	10.5	13.4
t_{PLZ}				10.5	13.4

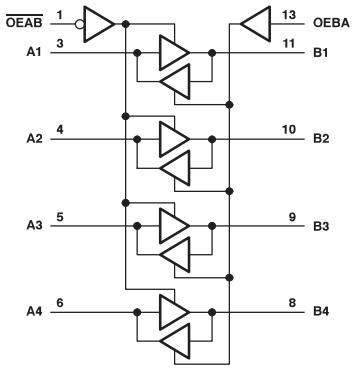
UNIT: ns

243

QUADRUPLE BUS TRANSCEIVERS

- Two-Way Asynchronous Communication Between Data Buses
- PNP Inputs Reduce DC Loading

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\overline{G}AB$	GBA	
L	L	A to B
H	H	B to A
H	L	Isolation
L	H	Latch A and B (A = B)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CCH}	MAX	38	25	44	0.08	0.16	0.16	mA
I_{CCL}	MAX	50	30	74	0.08	0.16	0.16	mA
I_{CCZ}	MAX	54	32	56	0.08	0.16	0.16	mA
I_{OH}	MAX	-15	-15	-	-	-6	-6	mA
I_{OL}	MAX	24	24	64	6	6	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A or B	A or B	MAX	18	11	7.5	25	27	33
t_{PHL}	A or B	A or B	MAX	18	11	6.5	25	27	33
t_{PZH}	$\overline{G}AB$	B	MAX	23	20	9	38	45	51
t_{PZL}				30	20	7.5	38	45	51
t_{PHZ}	$\overline{G}AB$	B	MAX	25	14	6.5	38	45	53
t_{PLZ}				20	22	9	38	45	53
t_{PZH}	GAB	A	MAX	23	20	10.5	38	45	51
t_{PZL}				30	20	8.5	38	45	51
t_{PHZ}	GAB	A	MAX	25	14	7	38	45	53
t_{PLZ}				20	22	11	38	45	53

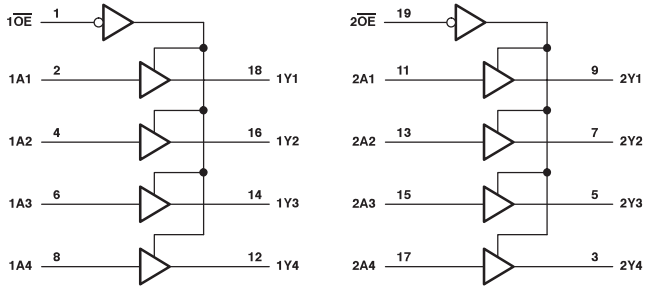
UNIT: ns

244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVT 3V	LVTH 3V	LVTT	LVTZ 3V	UNIT
I_{CCH}	MAX	27	160	17	17	34	60	0.08	0.16	0.08	0.16	40	40	0.25	0.19	0.19	0.19	0.225	mA
I_{CCL}	MAX	46	180	24	24	90	90	0.08	0.16	0.08	0.16	80	80	30	5	5	12	15	mA
I_{CCZ}	MAX	54	180	27	27	54	90	0.08	0.16	0.08	0.16	10	10	0.25	0.19	0.19	0.19	0.225	mA
I_{OH}	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-15	-32	-32	-32	-32	-32	mA
I_{OL}	MAX	24	64	24	48	64	64	6	6	6	6	64	64	64	64	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	UNIT
I_{CCH}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I_{CCL}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I_{CCZ}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	-24	-24	-24	mA
I_{OL}	MAX	24	24	24	24	24	24	8	8	8	16	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT
t_{PLH}	A	Y	MAX	18	9	10	10	6.2	6.2	29	33	35	38	5	5.3	4.6
t_{PHL}				18	9	10	10	6.2	6.5	29	33	35	38	5.5	6	4.6
t_{PZH}	$\overline{G}$	Y	MAX	23	12	20	20	9	6.7	38	-	44	-	8.7	9	5.1
t_{PZL}				30	15	20	20	7.5	8	38	-	44	-	8.9	9.4	6.1
t_{PHZ}	$\overline{G}$	Y	MAX	25	9	10	10	6	7	38	-	44	-	7.7	8	6.6
t_{PLZ}				20	15	13	13	9	7	38	-	44	-	8.9	9.8	5.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	LVTT	LVTZ 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V
t_{PLH}	A	Y	MAX	3.5	3.5	4.1	4.1	7.3	7.5	8.2	9.9	10	9.6	8.5	9.5	13.5
t_{PHL}				3.3	3.3	4.1	4.1	6.9	7.5	8.2	9.2	10	9.6	8.5	9.5	13.5
t_{PZH}	$\overline{G}$	Y	MAX	4.5	4.5	5.2	5.2	8.5	8	12	12.5	9.5	13.4	10.5	13	16
t_{PZL}				4.4	4.4	5.2	5.2	8.5	8.5	12	11.4	10.5	13.4	10.5	13	16
t_{PHZ}	$\overline{G}$	Y	MAX	4.4	4.4	5.6	5.6	7.3	9.5	12	10.4	10.5	13.4	10.5	13	18
t_{PLZ}				4.4	4.4	5.1	5.1	8.2	9.5	12	11.2	10.5	13.4	10.5	13	18

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 5V	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V
t_{PLH}	A	Y	MAX	8.5	5.9	5.9	5.9	2.8	2.8
t_{PHL}				8.5	5.9	5.9	5.9	2.8	2.8
t_{PZH}	$\overline{G}$	Y	MAX	10.5	7.6	7.6	7.6	4.5	4.5
t_{PZL}				10.5	7.6	7.6	7.6	4.5	4.5
t_{PHZ}	$\overline{G}$	Y	MAX	15.5	6.5	5.8	6.5	4.2	4.2
t_{PLZ}				15.5	6.5	5.8	6.5	4.2	4.2

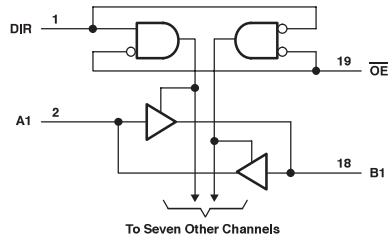
UNIT: ns

245

OCTAL BUS TRANSCEIVERS

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	ABTH	LVT 3V	LVTH 3V	LVTR 3V	UNIT
I_{CCH}	MAX	70	45	45	97	90	0.08	0.16	0.08	0.16	57	57	0.25	0.25	0.19	0.19	0.19	mA
I_{CCL}	MAX	90	55	55	143	120	0.08	0.16	0.08	0.16	90	90	30	30	5	5	12	mA
I_{CCZ}	MAX	95	58	58	123	110	0.08	0.16	0.08	0.16	15	15	0.25	0.25	0.19	0.19	0.19	mA
I_{OH} (A port)	MAX	-15	-15	-15	-15	-3	-6	-4	-6	-4	-3	-3	-32	-32	-32	-32	-12	mA
I_{OH} (B port)	MAX	-15	-15	-15	-15	-15	6	-4	-6	-4	-15	-15	-32	-32	-32	-32	-32	mA
I_{OL} (A port)	MAX	24	24	48	64	24	-6	4	6	4	24	24	64	64	64	64	32	mA
I_{OL} (B port)	MAX	24	24	48	64	64	6	4	6	4	64	64	64	64	64	64	32	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	UNIT
I_{CCH}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I_{CCL}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I_{CCZ}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I_{OH} (A port)	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	-24	-24	-24	mA
I_{OH} (B port)	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	-24	-24	-24	mA
I_{OL} (A port)	MAX	24	24	24	24	24	24	8	8	8	16	24	24	24	24	24	mA
I_{OL} (B port)	MAX	24	24	24	24	24	24	8	8	8	16	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	ABTH
t_{PLH}	A, B	B, A	MAX	12	10	10	7.5	7	26	33	28	39	7	7	3.6	3.6
t_{PHL}				12	10	10	7	7	26	33	28	39	7	7	3.9	3.9
t_{PZH}	$\overline{G}$	A, B	MAX	40	20	20	9	8	58	45	58	48	10.9	10.9	5.6	5.6
t_{PZL}				40	20	20	8.5	9	58	45	58	48	11.6	11.6	6.2	6.2
t_{PHZ}	$\overline{G}$	A, B	MAX	28	10	10	5.5	7.5	50	45	50	45	9.3	9.3	5.9	5.9
t_{PLZ}				25	15	15	9.5	7.5	50	45	50	45	9.1	9.1	4.5	4.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	A, B	B, A	MAX	3.5	3.5	9.5	7	8.5	10	8	10	8.5	9.5	13.5	8.5	6.3
t_{PHL}				3.5	3.5	6.9	7	8.5	9.1	9	10	8.5	9.5	13.5	8.5	6.3
t_{PZH}	$\overline{G}$	A, B	MAX	5.5	5.5	11.4	9	14	13.2	11	14	12	16	19	12	8.5
t_{PZL}				5.5	5.5	9.5	9.5	14	12.9	12	14	12	16	19	12	8.5
t_{PHZ}	$\overline{G}$	A, B	MAX	5.9	5.9	9.5	10	14	12.9	11	14.4	11	16.5	22	16	7.5
t_{PLZ}				5	5	10.4	10	14	13.9	11	14.4	11	16.5	22	16	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V
t_{PLH}	A, B	B, A	MAX	6.3	6.3	3.4	3.4
t_{PHL}				6.3	6.3	3.4	3.4
t_{PZH}	$\overline{G}$	A, B	MAX	8.5	8.5	5.5	5.5
t_{PZL}				8.5	8.5	5.5	5.5
t_{PHZ}	$\overline{G}$	A, B	MAX	7.5	7.5	5.5	5.5
t_{PLZ}				7.5	7.5	5.5	5.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTR 3V
t_{PLH}	A	B	MAX	4.2
	B	A		4.4
t_{PHL}	A	B	MAX	4.6
	B	A		4.1
t_{PZH}	$\overline{G}$	B	MAX	5.5
		A		6
t_{PZL}	$\overline{G}$	B	MAX	6.6
		A		6.4
t_{PHZ}	$\overline{G}$	B	MAX	6.1
		A		5.8
t_{PLZ}	$\overline{G}$	B	MAX	5.2
		A		5.2

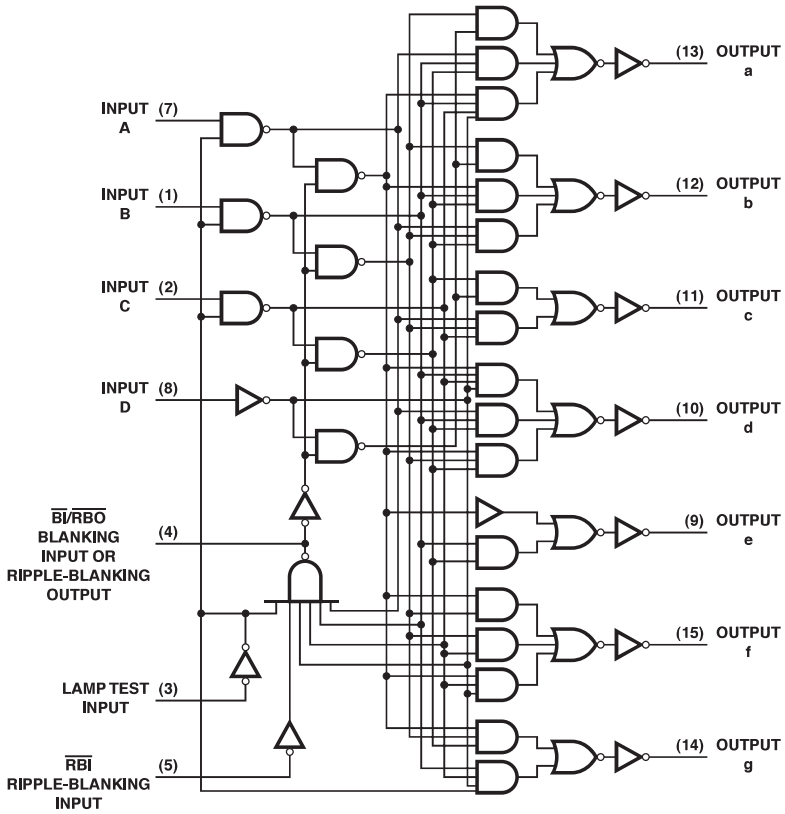
UNIT: ns

247

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS WITH RIPPLE BLANKING

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS					BI/RBO	OUTPUTS						
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	UNIT
I_{CC}		MAX	103	13	mA
V_O(off)	a thru g	MAX	15	15	V
I_O(on)		MAX	40	24	mA
I_{OH}	BI/RBO	MAX	-0,2	-0,05	mA
I_{OL}		MAX	8	3,2	mA

SWITCHING CHARACTERISTICS

PARAMETER		MAX or MIN	TTL	LS
toff	INPUT A	MIN	100	100
ton			100	100
toff	INPUT $\overline{RBI}$	MIN	100	100
ton			100	100

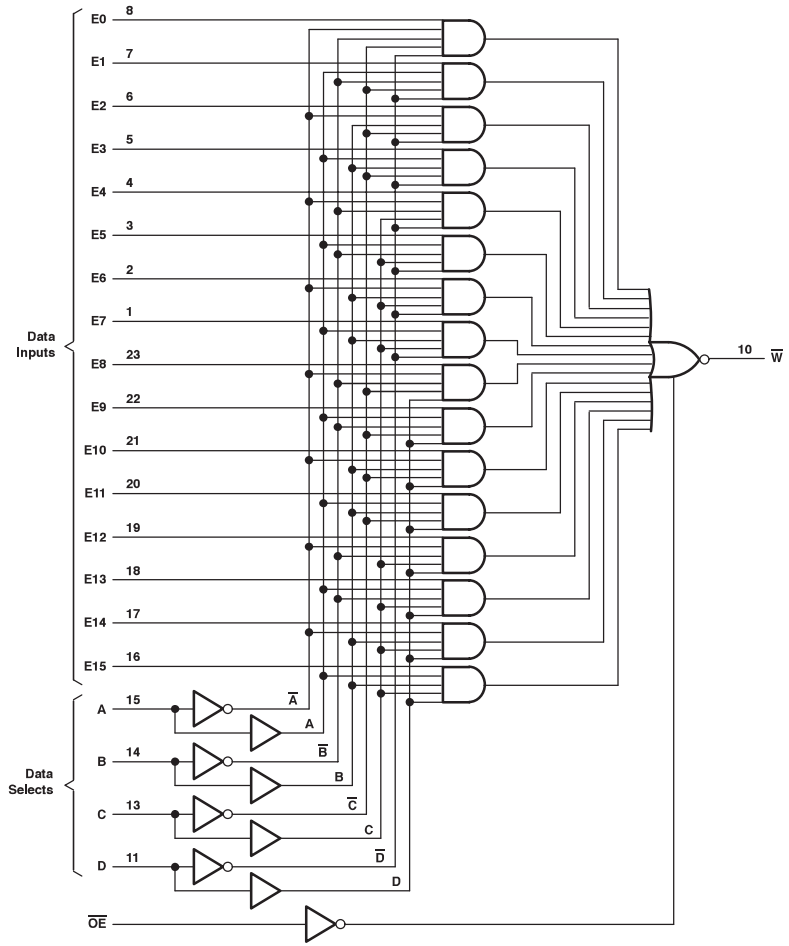
UNIT: ns

250

1-OF-16 DATA SELECTOR/MULTIPLEXER

- 4-Line to 1-Line Multiplexers That Can Select 1-of-16 Data Inputs
- Applications:
  - Boolean Function Generator
  - Parallel-to-Serial Converter
  - Data Source Selector
- Buffered 3-State Bus Driver Inputs Permit Multiplexing From n Lines to One Line
- 3-State Outputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUT
$\overline{G}$	A	B	C	D	EI	$\overline{W}$
L	L	L	L	L	E0	E0
L	H	L	L	L	E1	E1
L	L	H	L	L	E2	E2
L	H	H	L	L	E3	E3
L	L	L	H	L	E4	E4
L	H	L	H	L	E5	E5
L	L	H	H	L	E6	E6
L	H	H	H	L	E7	E7
L	L	L	L	H	E8	E8
L	H	L	L	H	E9	E9
L	L	H	L	H	E10	E10
L	H	H	L	H	E11	E11
L	L	L	H	H	E12	E12
L	H	L	H	H	E13	E13
L	L	H	H	H	E14	E14
L	H	H	H	H	E15	E15
H	X	X	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I_{CC}	MAX	50	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
t_{PLH}	DATA	$\overline{W}$	MAX	8
t_{PHL}				7
t_{PLH}	SELECT	$\overline{W}$	MAX	13
t_{PHL}				10.5
t_{PZH}	$\overline{G}$	$\overline{W}$	MAX	7
t_{PZL}				9
t_{PHZ}	$\overline{G}$	$\overline{W}$	MAX	6
t_{PLZ}				6.5

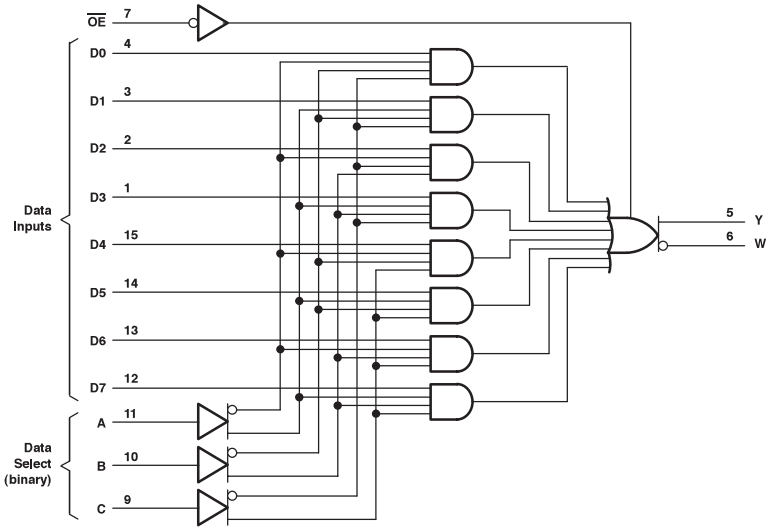
UNIT: ns

251

DATA SELECTORS/MULTIPLEXERS

- 3-State Version of '151
- 3-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	Z	$\overline{Z}$
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC	UNIT
I_{CC}	MAX	62	12	85	14	24	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-5.2	-2.6	-6.5	-2.6	-3	-6	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	24	24	6	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC
t_{PLH}	A, B, C	Y	MAX	45	45	18	18	9.5	51	74	63	18.2	18.2
t_{PHL}				45	45	19.5	24	7.5	51	74	63	18.2	18.2
t_{PLH}	A, B, C	W (CD74: $\overline{Y}$)	MAX	33	33	15	24	12.5	51	74	63	19.6	19.6
t_{PHL}				33	33	13.5	23	9	51	74	63	19.6	19.6
t_{PLH}	ANY D	Y	MAX	28	28	12	10	7	49	53	53	13.5	13.5
t_{PHL}				28	28	12	15	5	49	53	53	13.5	13.5
t_{PLH}	ANY D	W (CD74: $\overline{Y}$)	MAX	15	15	7	15	8	49	53	53	14.9	14.9
t_{PHL}				15	15	7	15	8	49	53	53	14.9	14.9
t_{PZH}	$\overline{G}$	Y	MAX	27	45	19.5	15	7	36	42	45	13.5	13.5
t_{PZL}				40	40	21	15	6.5	36	42	45	13.5	13.5
t_{PZH}	$\overline{G}$	W (CD74: $\overline{Y}$)	MAX	27	27	19.5	15	6	36	42	45	13.5	13.5
t_{PZL}				40	40	21	15	4.5	36	42	45	13.5	13.5
t_{PHZ}	$\overline{G}$	Y	MAX	8	45	8.5	10	8.5	49	42	45	13.5	13.5
t_{PLZ}				23	25	14	10	8	49	42	45	13.5	13.5
t_{PHZ}	$\overline{G}$	W (CD74: $\overline{Y}$)	MAX	8	55	8.5	10	5.5	49	42	45	13.5	13.5
t_{PLZ}				23	25	14	10	4.5	49	42	45	13.5	13.5

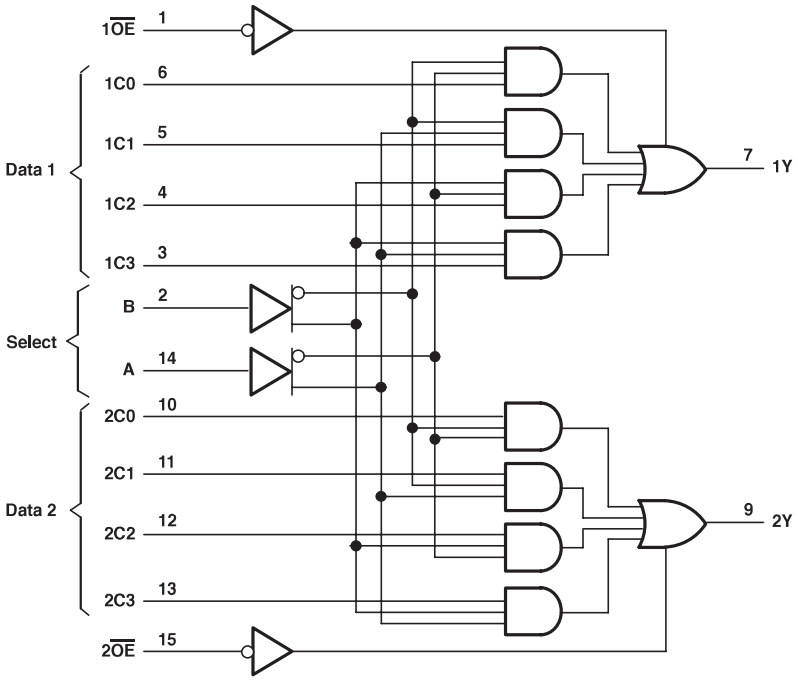
UNIT: ns

253

DUAL DATA SELECTORS/MULTIPLEXERS

- 3-State Version of '153
- Perform Parallel-to-Serial Conversion

Logic Diagram



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	14	14	33	23	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-2.6	-2.6	-15	-3	-6	-6	-4	-24	-24	mA
I_{OL}	MAX	8	24	48	24	6	6	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	DATA	Y	MAX	25	10	7.5	8	35	53	57	13.3	18
t_{PHL}				20	14	8	7	35	53	57	13.3	18
t_{PLH}	SELECT	Y	MAX	45	21	13.5	13	38	53	60	20	22
t_{PHL}				32	21	11.5	10	38	53	60	20	22
t_{PZH}	$\overline{G}$	Y	MAX	28	14	12.5	9	25	33	45	11.5	12.6
t_{PZL}				23	16	11.5	9	25	33	45	11.5	12.6
t_{PHZ}	$\overline{G}$	Y	MAX	41	10	6	6	38	45	45	11.5	12.6
t_{PLZ}				27	14	7	7	38	45	45	11.5	12.6

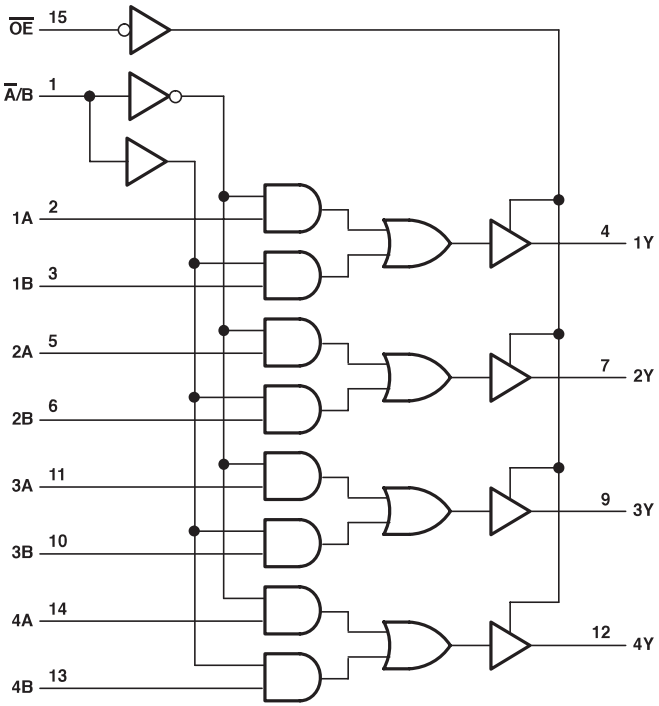
UNIT: ns

257

QUAD DATA SELECTORS/MULTIPLEXERS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OUTPUT CONTROL	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
I_{CC}	MAX	19	87	14	31.9	23	0.08	0.16	0.08	0.16	0.08	0.16	0.08	0.16	0.01	mA
I_{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-24	-24	-24	-24	-24	mA
I_{OL}	MAX	24	20	24	48	24	6	6	6	6	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
t_{PLH}	DATA	ANY	MAX	13	7.5	10	5.5	7	25	45	38	50	6.4	9.3	6.9	10.7	4.6
t_{PHL}				15	6.5	12	6	6.5	25	45	38	50	7.2	9.3	8.7	10.7	4.6
t_{PLH}	SELECT	ANY	MAX	21	15	18	11	15	25	53	38	57	7.2	13.4	8.2	15.4	6.4
t_{PHL}				24	15	22	10	9.5	25	53	38	57	7.9	13.4	9.4	15.4	6.4
t_{PZH}	G	Y	MAX	30	19.5	16	7.5	8.5	38	45	38	45	6.5	14.7	7.3	16.1	5.6
t_{PZL}				30	21	18	9.5	8.5	38	45	38	45	8.6	14.7	9.6	16.1	5.6
t_{PHZ}	G	Y	MAX	30	8.5	10	6.5	7	38	45	38	45	7.6	14.7	8.4	16.1	4.3
t_{PLZ}				25	14	15	7	7	38	45	38	45	7.6	14.7	8.5	16.1	4.3

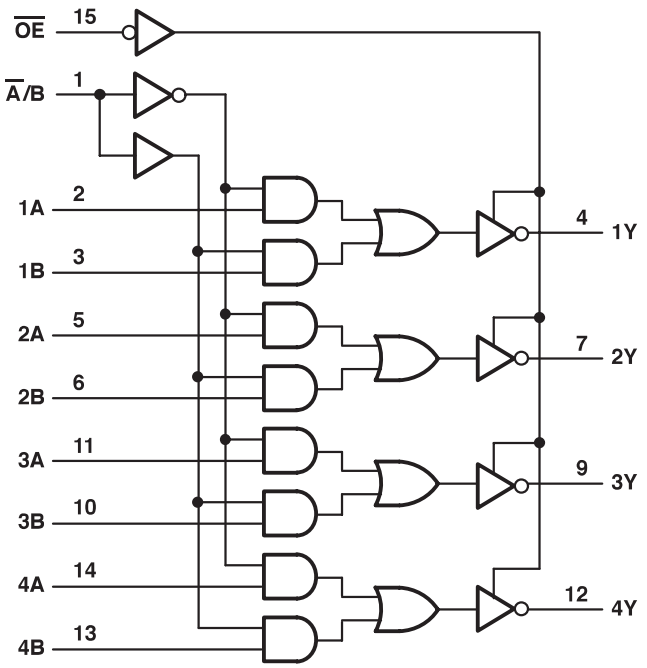
UNIT: ns

258

QUAD DATA SELECTORS/MULTIPLEXERS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT	UNIT
I_{CC}	MAX	16	87	13	25.2	23	0.08	0.16	0.16	0.16	mA
I_{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-24	mA
I_{OL}	MAX	8	20	24	48	24	6	6	6	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT
t_{PLH}	DATA	Y	MAX	12	6	8	5	6	25	24	34	10.7
t_{PHL}				17	6	7	4	5.5	25	24	34	10.7
t_{PLH}	SELECT	Y	MAX	21	12	25	9.5	9.5	29	35	43	15.4
t_{PHL}				24	12	20	10	11	29	35	43	15.4
t_{PZH}	$\overline{G}$	Y	MAX	30	19.5	18	8	8.5	38	35	35	16.1
t_{PZL}				30	21	18	10	8.5	38	35	35	16.1
t_{PHZ}	$\overline{G}$	Y	MAX	30	8.5	10	6	7	38	38	38	16.1
t_{PLZ}				25	14	18	6.5	7	38	38	38	16.1

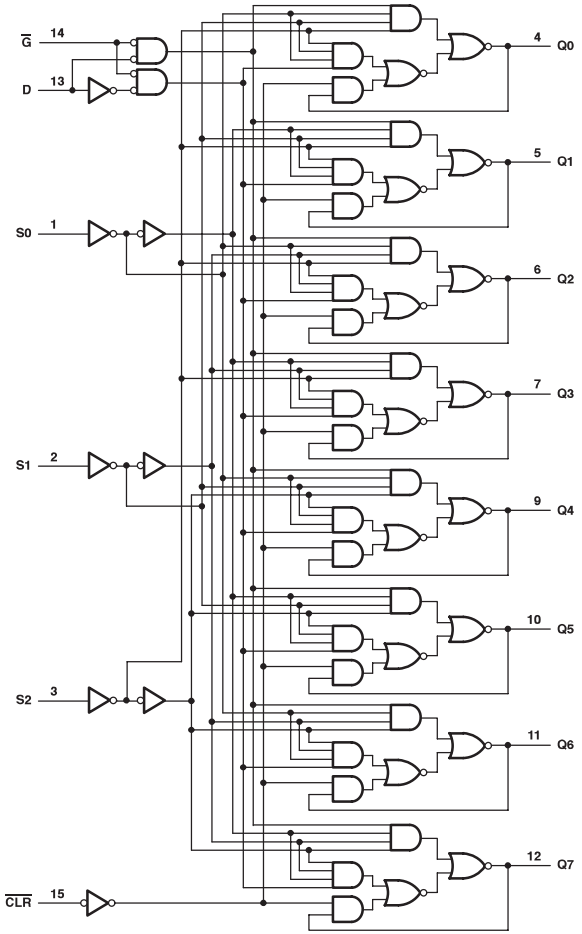
UNIT: ns

259

8-BIT ADDRESSABLE LATCHES

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

LATCH SELECTION

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	Qi0	Addressable latch
H	H	Qi0	Qi0	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	90	36	22	0.08	0.16	0.16	mA
I_{OH}	MAX	16	8	8	4	4	4	mA
I_{OL}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
tw	$\overline{G}$			MIN	15	17	15	20	21	27
	$\overline{CLR}$				15	10	10	20	21	27
tsu	DATA			MIN	15	20	15	19	24	26
	ADDRESS				5	17	15	19	24	26
th	DATA			MIN	0	0	0	5	0	0
	ADDRESS				20	0	0	5	0	0
t_{PLH}		$\overline{CLEAR}$	Any Q	MAX	25	18	12	38	47	59
t_{PHL}		DATA	Any Q	MAX	24	30	19	33	56	59
t_{PLH}					20	20	12	33	56	59
t_{PHL}		ADDRESS	Any Q	MAX	28	27	22	50	56	61
t_{PLH}					28	20	12	50	56	61
t_{PHL}		ENABLE	Any Q	MAX	20	24	20	43	51	57
t_{PHL}					20	24	13	43	51	57

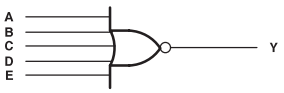
UNIT: ns

260

DUAL 5-INPUT POSITIVE-NOR GATES

● $Y = \overline{A + B + C + D + E}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	F	UNIT
I_{CC}	MAX	45	9.5	mA
I_{OH}	MAX	-1	-1	mA
I_{OL}	MAX	20	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
t_{PLH}	A, B, C, D, E	Y	MAX	5.5	6.5
t_{PHL}				6	4.5

UNIT: ns

265

QUAD COMPLEMENTARY-OUTPUT ELEMENTS

- $Y = \overline{A}$, W = A
- Y = AB, W = AB

Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	34	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tPLH	A or B		MAX	18
tPHL Y	A or B	Y	MAX	18
tPLH	A or B		MAX	18
tPHL Y	A or B	Y	MAX	18
tPLH -tPHL Y	A or B	with respect Y	MAX	3
tPHL -tPLH Y	A or B	with respect Y	MAX	3

UNIT: ns

266

QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

- $Y = \overline{A \oplus B}$

Logic Diagram

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	HC	UNIT
I_{CC}	MAX	13	0.02	mA
V_{OH}	MAX	5.5	Vcc	V
I_{OL}	MAX	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t_{PLH}	A or B Other Input Low	Y	MAX	30	31
t_{PHL}	A or B Other Input Low	Y	MAX	30	25
t_{PLH}	A or B Other Input High	Y	MAX	30	31
t_{PHL}	A or B Other Input High	Y	MAX	30	25

UNIT: ns

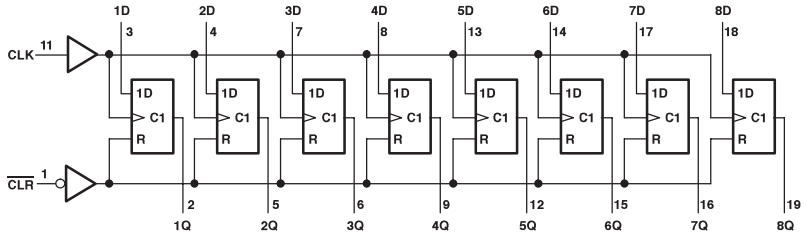
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

273

OCTAL D-TYPE FLIP-FLOPS

- Contain Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct-Clear Inputs

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	94	27	29	0.08	0.16	0.08	0.16	30	5	0.16	0.16	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-2.6	-4	-4	-4	-4	-32	-32	-24	-24	-8	-8	-6	-12	mA
I_{OL}	MAX	16	8	24	4	4	4	4	64	64	24	24	8	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC
fmax				MIN	30	30	35	21	20	16	16	150	150	100	85	70
t				MIN	16.5	20	14	20	24	25	30	3.3	3.3	5	6	5
tsu	DATA INPUT			MIN	20	20	10	25	18	25	18	2.5	2.3	2	2	4.5
	CLR INACVIVE			MIN	25	25	15	25	-	25	-	2	2.3	-	-	2
th				MIN	5	5	0	0	3	0	3	1.2	0	2	2	1
t_{PHL}		$\overline{CLEAR}$	ANY Q	MAX	27	27	18	40	45	42	48	7.4	4.9	13.5	13.5	12
t_{PLH}		CLOCK	ANY Q	MAX	27	27	12	40	45	42	45	6.5	4.8	13.5	13.5	12.5
t_{PHL}					27	27	15	40	45	42	45	7.3	4.3	13.5	13.5	12.5

PARAMETER		INPUT	OUTPUT	MAX or MIN	AHCT	LV 3V	LV 5V
fmax				MIN	45	45	70
t				MIN	6.5	6.5	5
tsu	DATA INPUT			MIN	5	6.5	4.5
	CLR INACVIVE			MIN	2.5	2.5	2
th				MIN	0	2	1
t_{PHL}		$\overline{CLEAR}$	ANY Q	MAX	12.6	19.5	12
t_{PLH}		CLOCK	ANY Q	MAX	9.8	19.5	12.5
t_{PHL}					11	19.5	12.5

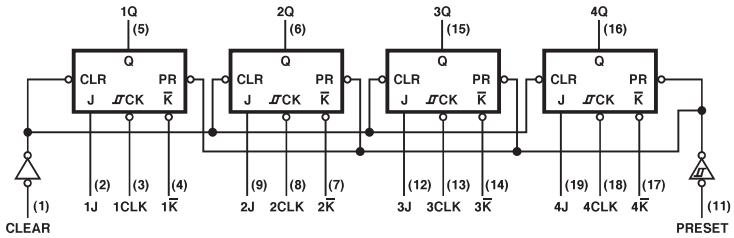
UNIT fmax : MHz, other : ns

276

QUAD J-$\overline{K}$ FLIP-FLORS

- Separate Negative-Edge-Triggered Clocks
- Fully Buffered Outputs

Logic Diagram



FUNCTION TABLE

COMMON INPUTS		INPUTS			OUTPUT
PRESET	CLEAR	CLOCK	J	K	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	H†
H	H	↓	L	H	Q_0
H	H	↓	H	H	H
H	H	↓	L	L	L
H	H	↓	H	L	TOGGLE
H	H	H	X	X	Q_0

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	81	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL
fmax				MIN	35
tw	CLOCK high			MIN	13.5
	CLOCK low				15
tsu	J, K			MIN	3
	$\overline{CLR}$, $\overline{PR}$				10
th				MIN	10
t_{PLH}		$\overline{PRESET}$	Q	MAX	25
t_{PHL}		$\overline{CLEAR}$	Q	MAX	30
t_{PLH}		CLOC	Q	MAX	30
t_{PHL}					30

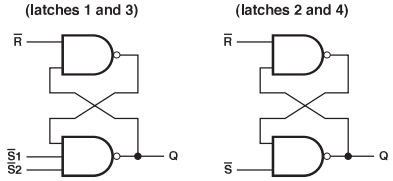
UNIT fmax : MHz, other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

279

QUAD $\overline{S}$-$\overline{R}$ LATCHES

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	30	7	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
$t_{\_\_}$			MIN	20	20
t_{PLH}	$\overline{S}$	Q	MAX	22	22
t_{PHL}				15	21
t_{PHL}	$\overline{R}$		MAX	27	27

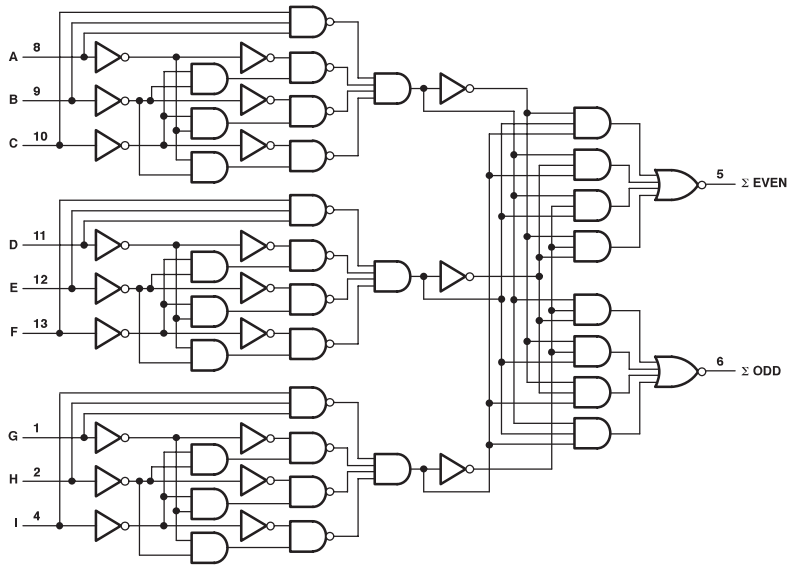
UNIT: ns

280

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity

Logic Diagram



FUNCTION TABLE

NO. OF INPUTS A–I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	27	105	16	35	35	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-0.4	-1	-2.6	-2	-1	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	8	20	24	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	DATA	S EVEN	MAX	50	21	20	12	10	52	60	63	20	21.6
t_{PHL}				45	18	20	11	11	52	60	63	20	21.6
t_{PLH}	DATA	S ODD	MAX	35	21	20	12	10	52	60	68	21	21.6
t_{PHL}				50	18	22	11.5	11	52	60	68	21	21.6

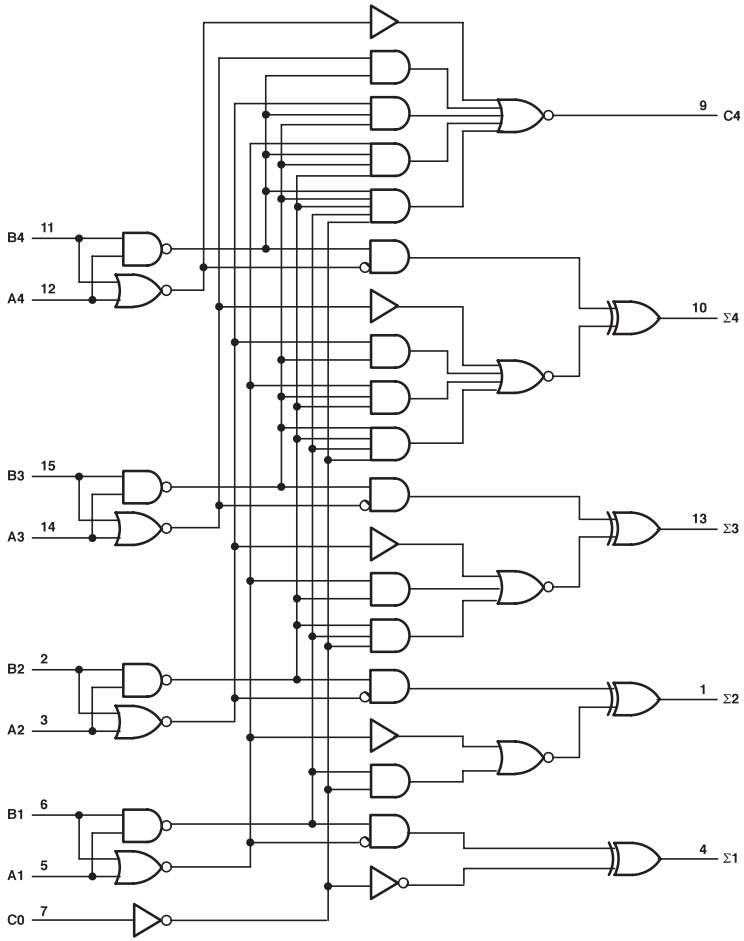
UNIT: ns

283

4-BIT BINARY FULL ADDERS

- Full-Carry Look-Ahead Across the Four Bits

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUTS					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
A3	B3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}		MAX	110	39	160	55	0.16	0.16	0.16	0.16	mA
I_{OH}	Any output except C4	MAX	-0.8	-0.4	-1	-1	-4	-4	-24	-24	mA
	C4	MAX	-0.4	-0.4	-0.5	-1	-4	-4	-24	-24	
I_{OL}	Any output except C4	MAX	16	8	20	20	4	4	24	24	mA
	C4	MAX	8	8	10	20	4	4	24	24	

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	C0	S	MAX	21	24	18	10.5	69	47	17.6	17.6
t_{PHL}			MAX	21	24	18	10.5	69	47	17.6	17.6
t_{PLH}	Ai or Bi	Si	MAX	24	24	18	10.5	63	69	18.2	18.2
t_{PHL}			MAX	24	24	18	10.5	63	69	18.2	18.2
t_{PLH}	C0	C4	MAX	14	17	11	8.5	59	80	17.6	17.6
t_{PHL}			MAX	16	22	11	8	59	80	17.6	17.6
t_{PLH}	Ai or Bi		MAX	14	17	12	8.5	59	72	17.6	17.6
t_{PHL}			MAX	16	17	12	8	59	72	17.6	17.6

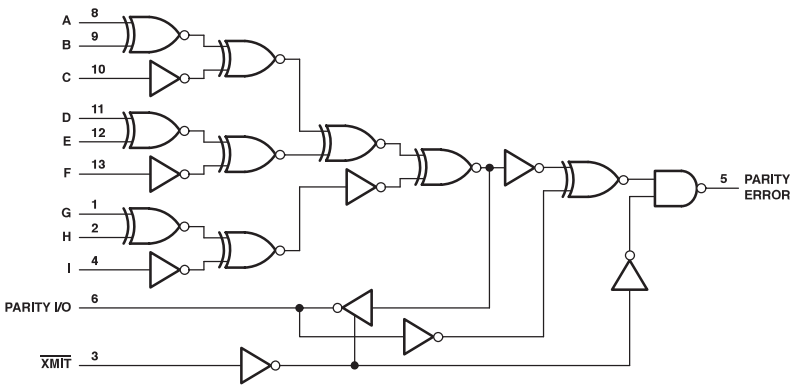
UNIT: ns

286

9-BIT PARITY GENERATOR/CHECKER WITH BUS DRIVER PARITY I/O PORT

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

NUMBER OF INPUTS (A–I) THAT ARE HIGH	$\overline{XMIT}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h h	h l	H L
1, 3, 5, 7, 9	h h	h l	L H

h = high input level l = low input level
H = high output level L = low output level

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AS	AC 11	ACT 11	UNIT
I_{CC}		MAX	50	0.08	0.08	mA
I_{OH}	Parity error	MAX	-2	-24	-24	mA
	Parity I/O	MAX	-15	-24	-24	mA
I_{OL}	Parity error	MAX	20	24	24	mA
	Parity I/O	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	AC 11	ACT 11
t_{PLH}	A to I	Parity I/O	MAX	15	9	10.4
t_{PHL}				14	107	12
t_{PLH}	A to I	Parity error	MAX	16.5	10	11.3
t_{PHL}				16.5	12	12.9
t_{PLH}	Parity I/O	Parity error	MAX	9	6.2	7.7
t_{PHL}				9	7.9	9.1
t_{PZH}	$\overline{XMIT}$	Parity I/O	MAX	13	5.3	7.3
t_{PZL}				16	8.9	11.4
t_{PHZ}				11.5	6.5	8.5
t_{PLZ}				10	6.3	7.8

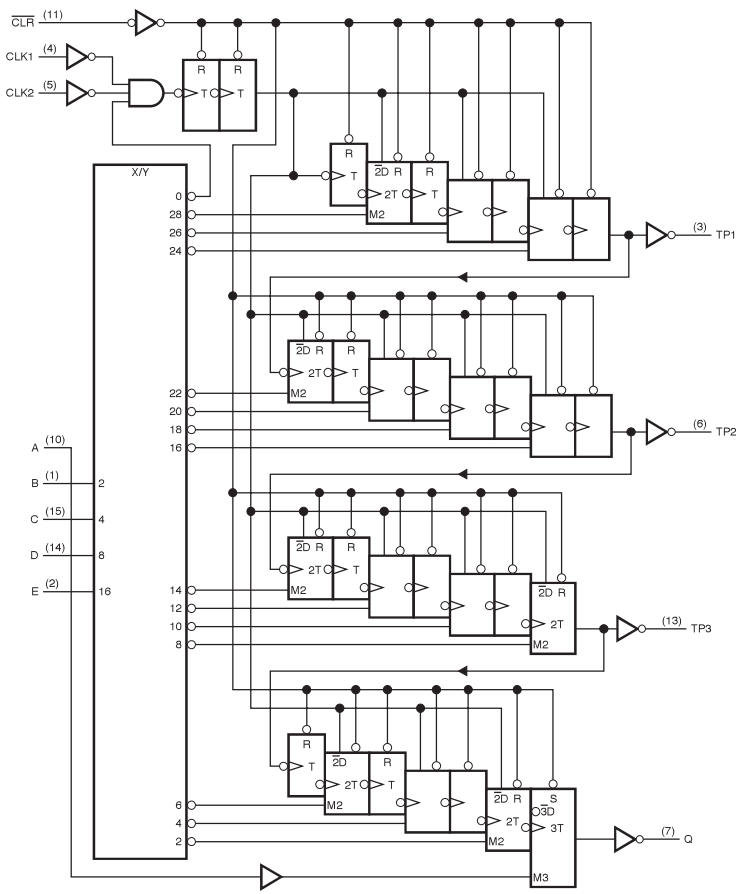
UNIT: ns

292

PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER

- Digitally Programmable from 2^2 to 2^{31}
- Easily Expandable
- Applications:
  - Frequency Division
  - Digital Timing

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↓	L	Count
H	L	↓	Count
H	H	X	Inhibit
H	X	H	Inhibit

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	75	mA
I_{OH} (Q only)	MAX	-1.2	V
I_{OL} (Q only)	MAX	24	mA

SWITCHING CHARACTERISTICS

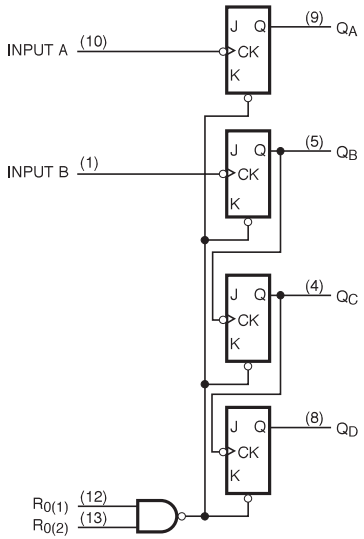
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax	CLK		MIN	30
t_{PLH}	CLK	Q	MAX	90
t_{PHL}	CLK	Q	MAX	120
t_{PHL}	$\overline{CLR}$	$\overline{Q}$	MAX	65

UNIT fmax : Hz, other : ns

293

4-BIT BINARY COUNTERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

COUNT SEQUENCE

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE: Output Q_A is connected to input B.

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUTS			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	39	15	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax		A	QA	MIN	32	32
		B	QB	MIN	16	16
tw	A	A, B		MIN	15	15
	B				30	30
	Reset				15	15
tsu				MIN	25	25
t_{PLH}		A	QA	MAX	16	16
t_{PHL}					18	18
t_{PLH}		A	QB	MAX	70	70
t_{PHL}					70	70
t_{PLH}		B	QB	MAX	16	16
t_{PHL}					21	21
t_{PLH}		B	QC	MAX	32	32
t_{PHL}					35	35
t_{PLH}		B	QD	MAX	51	51
t_{PHL}					51	51

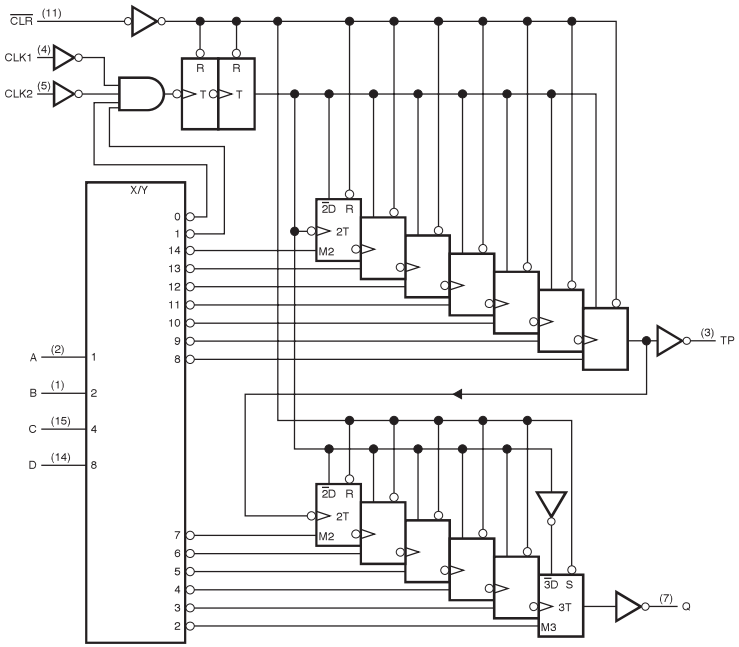
UNIT fmax : Hz, other : ns

294

PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER

- Digitally Programmable from 2^2 to 2^{15}
- Easily Expandable
- Applications
  - Frequency Division
  - Digital Timing

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1024	2^4	16
H	L	H	H	2^{11}	2048	2^5	32
H	H	L	L	2^{12}	4096	2^6	64
H	H	L	H	2^{13}	8192	2^7	128
H	H	H	L	2^{14}	16384	2^8	256
H	H	H	H	2^{15}	32768	2^9	512

RECOMMENDED OPERATING CONDITIONS

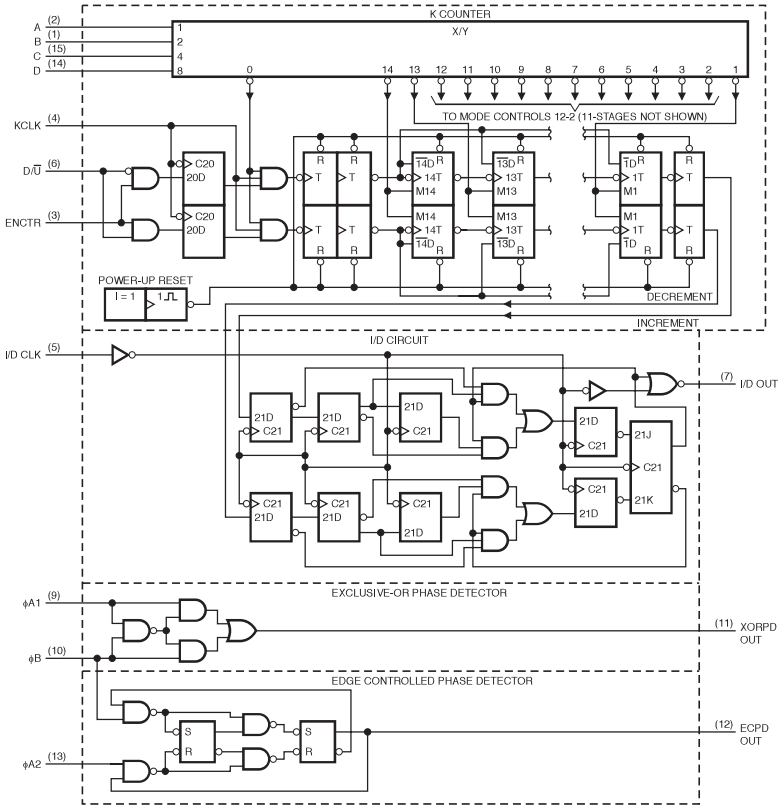
PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	50	mA
I_{OH}	MAX	-1.2	V
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax	CLK		MIN	30
tw	CLK 1 or 2		MIN	16
	CLR		MIN	35
t_{PLH}	CLK 1 or 2	Q	MAX	90
t_{PHL}				120
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	MAX	65

UNIT fmax : Iz, other : ns

Logic Diagram



FUNCTION TABLES

K COUNTER FUNCTION TABLE (DIGITAL CONTROL)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^2
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

EXCLUSIVE OR PHASE DETECTOR

ϕA1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR

ϕA2	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT	UNIT
I_{CC}	MAX	120	0.16	0.16	0.08	mA
I_{OH} (I/D OUT)	MAX	-1	-6	-4	-24	mA
I_{OH} (XOR, ECPD)	MAX	-0.4	-6	-4	-24	mA
I_{OL} (I/D OUT)	MAX	24	6	4	24	mA
I_{OL} (XOR, ECPD)	MAX	8	6	4	24	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT		OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT
fmax		K CLK		I/D OUT	MIN	32	20	20	45
		I/D CLK		I/D OUT		16	13	13	35
tw	K CLK				MIN	16	24	24	8
	I/D CLK					33	38	38	9
tsu	D/$\overline{U}$				MIN	30	30	30	17
	ENCLR					31	30	30	16
th	D/$\overline{U}$				MIN	0	0	0	7
	ENCLR					0	0	0	6
t_{PLH}		I/D CLK		I/D OUT	MAX	25	53	53	24
t_{PHL}						35	53	53	24
t_{PLH}		↑ A1 or B	other input low	X or OUT	MAX	15	45	45	22
			other input high			25	45	45	22
t_{PHL}		↓ A1 or B	other input low	X or OUT		25	45	45	22
			other input high			25	45	45	22
t_{PLH}		↑ B		ECPD OUT	MAX	30	60	60	30
t_{PHL}		↓ A2		ECPD OUT		30	60	60	30

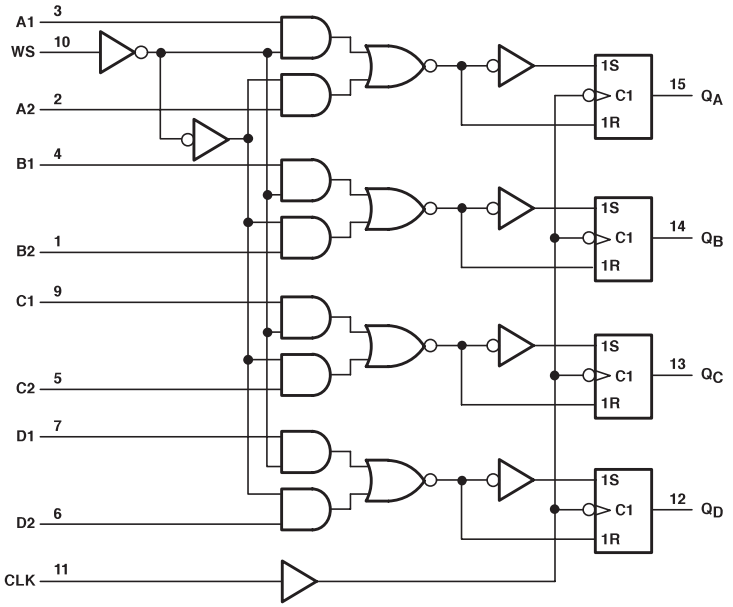
UNIT fmax : MHz, other : ns

298

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

● Outputs Storage Register

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

† a1, a2, etc. = the level of steady-state input at A1, A2, etc.
QA0, QB0, etc. = the level of QA, QB, etc. entered on the most recent O transition of CLK

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	AS	SN74 HC	UNIT
I_{CC}	MAX	65	21	36	0.08	mA
I_{OL}	MAX	16	8	20	4	mA
I_{OH}	MAX	-0.8	-0.4	-2	-4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	AS	SN74 HC
t				MIN	20	20	8	27
t_{su}	Data			MIN	15	15	4.5	21
	Word Select				25	25	13	21
t_h	Data			MIN	5	5	3.5	0
	Word Select				0	0	1	0
t_{PLH}		CLK	GA to GD	MAX	27	27	9	31
t_{PHL}					32	32	11	31

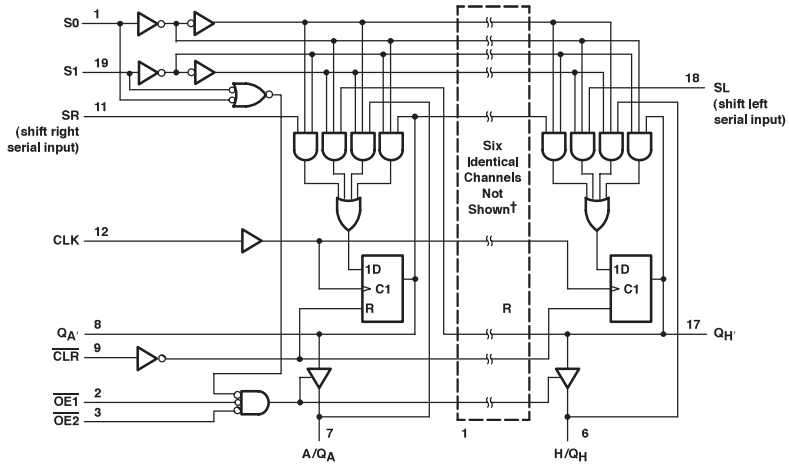
UNIT: ns

299

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- Operate with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	$\overline{OE1}$†	$\overline{OE2}$†	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a...h=the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputsare isolated from the I/O terminals.
† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operationor clearing of the register is not affected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}		MAX	53	225	40	95	0.16	0.16	0.16	0.16	mA
I_{OH}	Q_A thru Q_H	MAX	-2.6	-6.5	-2.6	-3	-6	-4	-24	-24	mA
	$Q_{A'}$ or $Q_{H'}$		-0.4	-0.5	-0.4	-1	-4	-4	-24	-24	
I_{OL}	Q_A thru Q_H	MAX	24	20	24	24	6	4	24	24	mA
	$Q_{A'}$ or $Q_{H'}$		8	6	8	20	4	4	24	24	

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax				MIN	20	50	30	70	20	16	95	90
t	CLK high			MIN	30	10	16.5	7	24	30	5.2	5.5
	CLK low				10	10	16.5	7	24	30	5.2	5.5
	$\overline{CLR}$				20	10	10	7	15	22	5	5
tsu	DATA "H"			MIN	20	7	16	5.5	36	30	4.5	4.5
	DATA "L"				20	5	6	5.5	36	30	4.5	4.5
	SELECT				35	15	20	8.5	36	41	9	9
	$\overline{CLR}$ INACTIVE				20	10	15	7	-	-	-	-
th	DATA			MIN	0	5	0	2	0	0	0	0
	SELECT				10	5	0	0	0	0	0	0
t_{PLH}		CLK	$Q_{A'}$ or $Q_{B'}$	MAX	33	20	15	10	60	68	12.9	12.9
t_{PHL}					39	20	18	9.5	60	68	12.9	12.9
t_{PLH}		CLK	Q_A thru Q_H	MAX	25	21	13	10	60	68	13.5	14.5
t_{PHL}					39	21	19	12	60	68	13.5	14.5
t_{PHL}		$\overline{CLR}$	$Q_{A'}$ or $Q_{H'}$	MAX	40	21	22	10.5	60	69	11.2	12.2
t_{PHL}		$\overline{CLR}$	Q_A thru Q_H		40	24	22	15	60	69	13.9	18.6
t_{PZH}		$\overline{OE1}$, $\overline{OE2}$	Q_A thru Q_H	MAX	21	18	16	9	47	48	14.9	14.9
t_{PZL}					30	18	22	11	39	45	14.9	14.9
t_{PHZ}		$\overline{OE1}$, $\overline{OE2}$	Q_A thru Q_H	MAX	20	12	8	7	56	56	14.9	14.9
t_{PLZ}					15	12	15	6.5	47	48	14.9	14.9

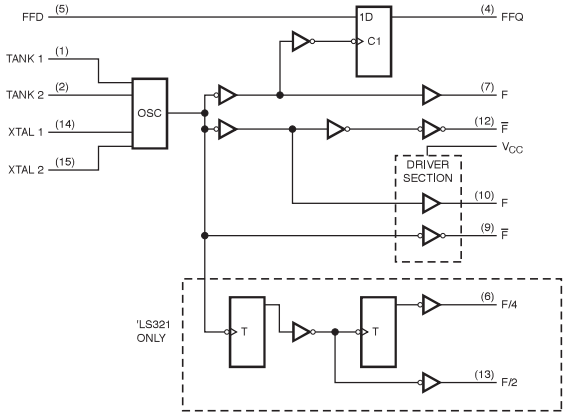
UNIT fmax : MHz, other : ns

321

CRYSTAL-CONTROLLED OSCILLATOR

- Crystal-Controlled Oscillator Operation from 1MHz to 20MHz
- Complementary Outputs

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	75	mA
I_{OH}	F' or $\overline{F}$'	MAX	-24	mA
	F, $\overline{F}$, F/2, F/4	MAX	-0.4	mA
I_{OL}	F' or $\overline{F}$'	MAX	24	mA
	F, $\overline{F}$, F/2, F/4	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax		F/2	MIN	10
		F/4	MAX	5
		ANY	MIN	20
tr		F',F'	MAX	14
		ANY	MAX	40
tf		F',F'	MAX	10
		ANY	MAX	20

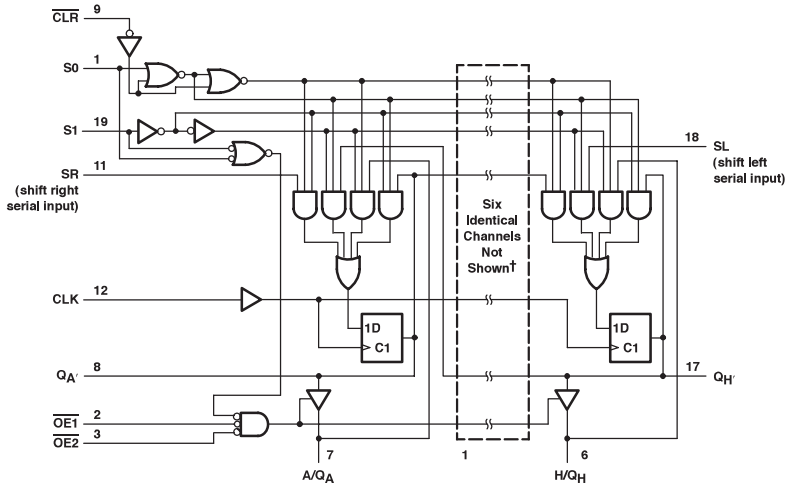
UNIT fmax : MHz, other : ns

323

8-BIT BIDIRECTIONAL SHIFT/STORAGE REGISTERS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram



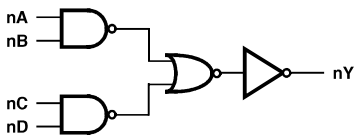
† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

4002

DUAL 4-INPUT POSITIVE-NOR GATES

● $Y = \overline{A + B + C + D}$

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

NOTES:
H = High Voltage Level
L = Low Voltage Level
X = Irrelevant

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	0.02	0.04	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

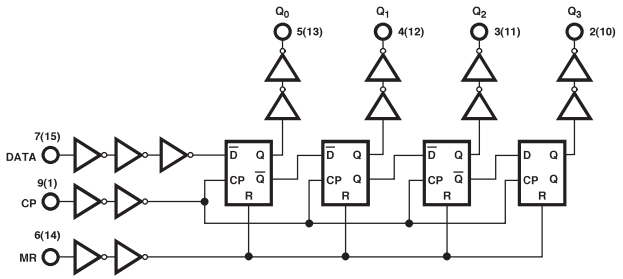
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
t_{PLH}	A, B, C, D	Y	MAX	28	30
t_{PHL}			MAX	28	30

UNIT:ns

4015

DUAL 4-STAGE STATIC SHIFT REGISTER

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT			
CP	D	R	Q_0	Q_1	Q_2	Q_3
↑	l	L	L	q'_0	q'_1	q'_2
↑	h	L	H	q'_0	q'_1	q'_2
↓	X	L	q'_0	q'_1	q'_2	q'_3
X	X	H	L	L	L	L

NOTES:
H = High Voltage Level
h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition
X = Don't Care.
↑ = Low to High Clock Transition
↓ = High to Low Clock Transition
q'_n = Lower case letters indicate the state of the referenced output one set-up time prior to the Low to High clock transition.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
f_{max}			MIN	45
t_W	Clock		MIN	24
	MR			45
t_{SUL}	Data-In to CP		MIN	18
t_{SUH}			MIN	18
t_H	Data-In to CP		MIN	0
t_{PLH}	Clock	Qn	MAX	54
t_{PHL}				54
t_{PLH}	MR	Qn (Clock High)	MAX	83
t_{PHL}				83
t_{PLH}	MR	Qn (Clock Low)	MAX	98
t_{PHL}				98

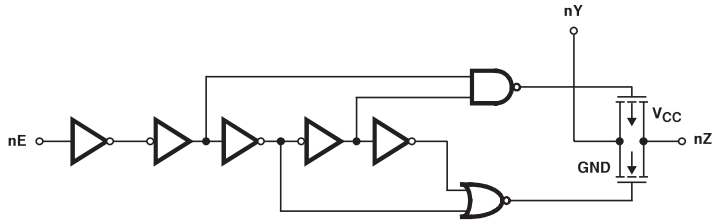
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4016

QUAD BILATERAL SWITCH

Logic Diagram



FUNCTION TABLE

INPUT nE	SWITCH
L	OFF
H	ON

NOTES:
H = High Level Voltage
L = Low Level Voltage

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.32	mA

SWITCHING CHARACTERISTICS

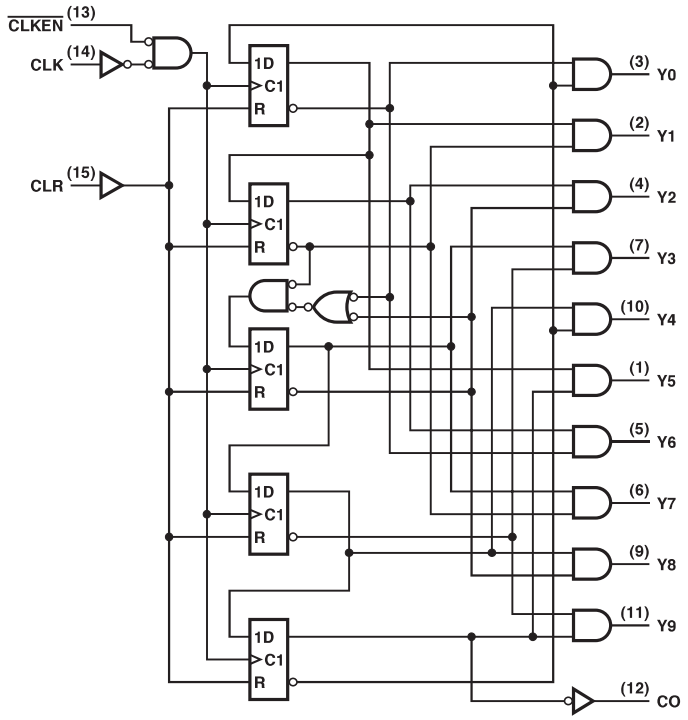
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_{PLH}	Switch In	Switch Out	MAX	18
t_{PHL}				18
t_{PZH}	En	Z	MAX	57
t_{PZL}				57
t_{PHZ}	En	Z	MAX	44
t_{PLZ}				44

UNIT:ns

4017

DECADE COUNTERS/DRIVERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS			OUTPUT
CLK	$\overline{CLKEN}$	CLR	STATE†
L	X	L	No Change
X	H	L	No Change
X	X	H	"0" = H, "1"-"9" = L
↑	L	L	Increments Counter
↓	X	L	No Change
X	↑	L	No Change
H	↓	L	Increments Counter

NOTES:
H = High Level
L = Low Level
↑ = High to Low Transition
↓ = Low to High Transition
X = Don't Care
† If n < 5 TC = H, Otherwise = L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	0.08	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
f_{max}			MIN	25	20
t_w	CLK (CP)		MIN	20	24
	CLR (MR) H			20	24
t_{su}	$\overline{CLKEN}$ to CLK ($\overline{CE}$ to CP)		MIN	13	22
	CLK Inactive			13	-
t_h	$\overline{CLKEN}$ to CLK ($\overline{CE}$ to CP)		MIN	5	0
t_{PLH}	CLK (CP)	Y, CO (0 to 9, TC)	MAX	58	69
t_{PHL}				58	69
t_{PLH}	$\overline{CLKEN}$ ($\overline{CE}$)	Y, CO (0 to 9, TC)	MAX	63	75
t_{PHL}				63	75
t_{PLH}	CLR (MR)	Y (0 to 9)	MAX	58	69
t_{PHL}				58	69
t_{PLH}	CLR (MR)	CO (TC)	MAX	-	69
t_{PHL}				58	69

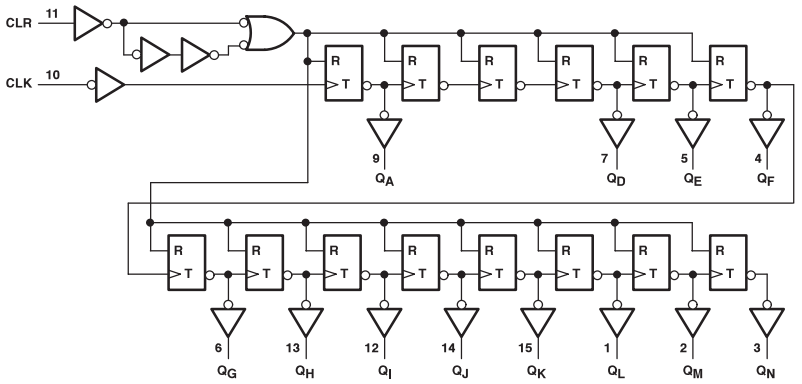
UNIT f_{max} : MHz, other : ns

4020

14-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4020
- V_{CC}: 2V to 6V

Logic Diagram



FUNCTION TABLE

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, =• •Transition from Low to High Level, • = Transition from High to Low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

SWITCHING CHARACTERISTICS

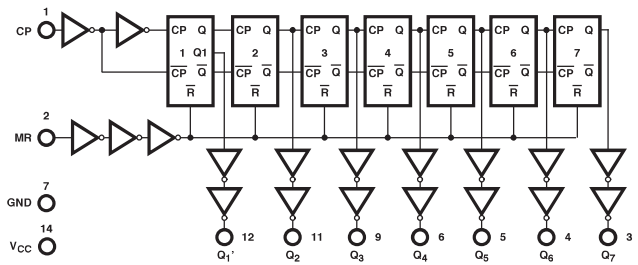
PARAMETER		INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
f_{max}				MIN	22	20	16
t_w	CLK			MIN	23	24	30
	CLR high				18	24	30
t_{su}	CLK	CLR inactive before CLI		MIN	15	-	-
t_{PLH}		CLK	Q_A	MAX	38	42	60
t_{PHL}					38	42	60
t_{PHL}		CLR	Any	MAX	35	51	60

UNIT fmax : MHz other : ns

4024

7-STAGE BINARY COUNTERS

Logic Diagram



FUNCTION TABLE

CLK	CLR	OUTPUT STATE
↓	L	No Change
↑	L	Advance to Next State
X	H	All outputs Are Low

NOTES:
H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition form Low to High Level, ↓ = Transition High to Low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
f_{max}			MIN	22	20	16
t_w	CLK (CP)		MIN	23	24	30
	CLR (MR) H			20	24	30
t_{su}	CLR iow before CLK		MIN	20	-	-
t_{PLH}	CLK (CP)	QA (Q1)	MAX	30	42	60
t_{PHL}				30	42	60
t_{PLH}	CLR (MR)	any Q	MAX	-	51	60
t_{PHL}				33	51	60

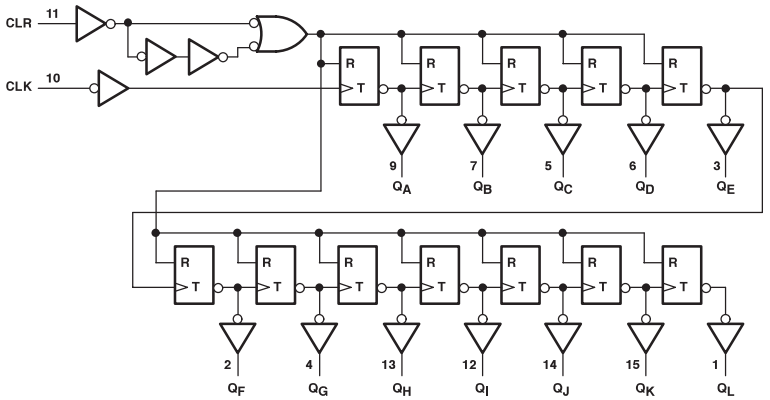
UNIT f_{max} : MHz, other : ns

4040

12-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4040
- V_{CC}: 2V to 6V

Logic Diagram



FUNCTION TABLE

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
f_{max}				MIN	22	20	16	50	80
t_w	CLK			MIN	23	24	30	5	5
	CLR high				18	24	30	5	5
t_{su}	CLK	CLR inactive before CLI		MIN	15	-	-	5	5
t_{PLH}		CLK	QA	MAX	38	42	60	17.5	10.5
t_{PHL}					38	42	60	17.5	10.5
t_{PHL}		CLR	Any	MAX	35	51	60	18.5	12

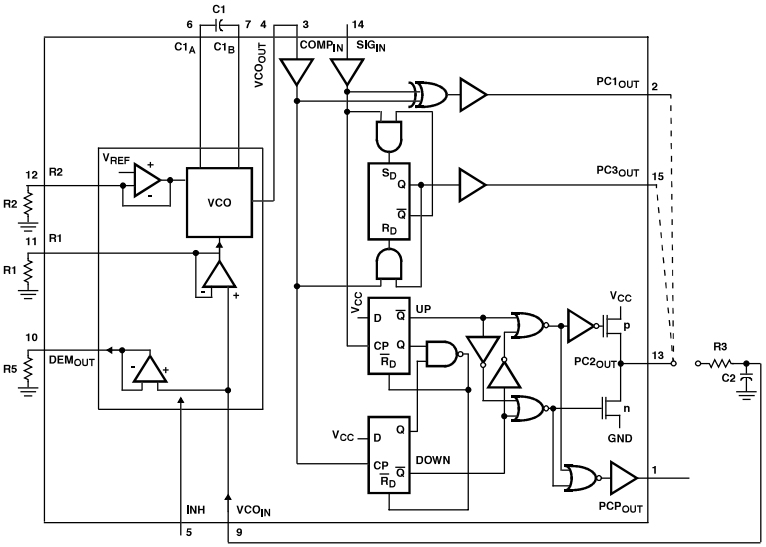
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4046

PHASE-LOCKED-LOOP WITH VCO

Logic Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	Phase Comparator Pulse Output
2	$PC1_{OUT}$	Phase Comparator 1 Output
3	$COMP_{IN}$	Comparator Input
4	VCO_{OUT}	VCO Output
5	INH	Inhibit Input
6	$C1_A$	Capacitor C1 Connection A
7	$C1_B$	Capacitor C1 Connection B
8	GND	Ground (0V)
9	VCO_{IN}	VCO Input
10	DEM_{OUT}	Demodulator Output
11	R_1	Resistor R1 Connection
12	R_2	Resistor R2 Connection
13	$PC2_{OUT}$	Phase Comparator 2 Output
14	SIG_{IN}	Signal Input
15	$PC3_{OUT}$	Phase Comparator 3 Output
16	V_{CC}	Positive Supply Voltage

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{PLH}	SIG_{IN}	PCI_{OUT}	MAX	60	68
t_{PHL}	$COMP_{IN}$			60	68
t_{PLH}	SIG_{IN}	PCP_{OUT}	MAX	90	102
t_{PHL}	$COMP_{IN}$			90	102
t_{PLH}	SIG_{IN}	$PC3_{OUT}$	MAX	74	87
t_{PHL}	$COMP_{IN}$			74	87
t_{TLH}	A	$\overline{Y}$	MAX	22	22
t_{THL}				22	22
t_{PZH}	SIG_{IN}	$PC2_{OUT}$	MAX	80	90
t_{PZL}	$COMP_{IN}$			80	90
t_{PLZ}	SIG_{IN}	$PC2_{OUT}$	MAX	95	102
t_{PHZ}	$COMP_{IN}$			95	102

UNIT:ns

4049

HEX INVERTING BUFFERS

Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_{PLH}	nA	$n\overline{Y}$	MAX	26
t_{PHL}				26

UNIT:ns

4050

HEX NON-INVERTING BUFFERS

Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

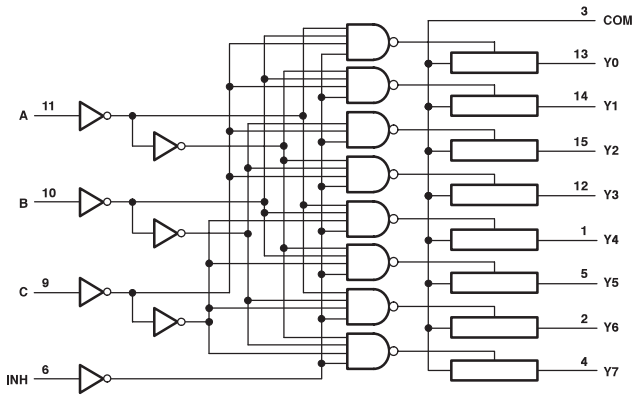
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_{PLH}	nA	nY	MAX	26
t_{PHL}				26

UNIT:ns

4051

8-CHANNEL ANALOG MULTIPLEXERS / DEMULTIPLEXERS

Logic Diagram



FUNCTION TABLE

INPUTS				ON
INH	C	B	A	CHANNEL
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	-	0.02	mA

SWITCHING CHARACTERISTICS

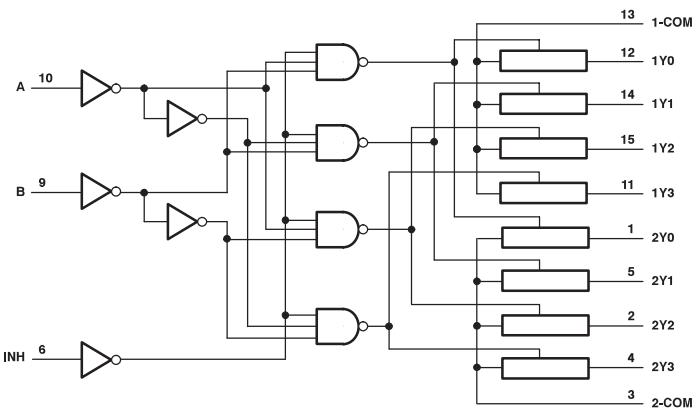
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	COM or Yn	Yn or COM	MAX	18	18	12	8
t_{PHL}				18	18	12	8
t_{PZH}	INH	COM or Yn	MAX	68	83	25	18
t_{PZL}				68	83	25	18
t_{PHZ}	INH	COM or Yn	MAX	68	68	25	18
t_{PLZ}				68	68	25	18

UNIT: ns

4052

DUAL 4-CHANNEL ANALOG MULTIPLEXERS / DEMULTIPLEXERS

Logic Diagram



FUNCTION TABLE

INPUTS			ON
INH	B	A	CHANNEL
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	-	0.02	mA

SWITCHING CHARACTERISTICS

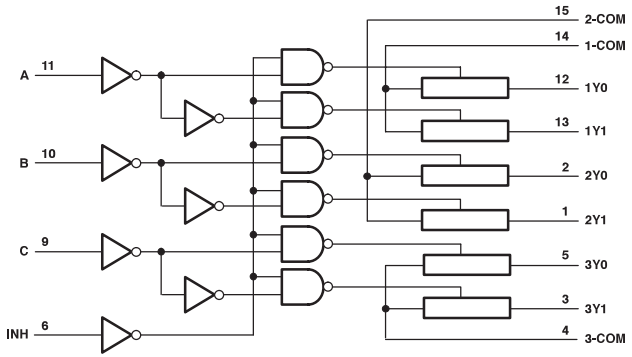
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	COM or Yn	Yn or COM	MAX	18	18	12	8
t_{PHL}				18	18	12	8
t_{PZH}	INH	COM or Yn	MAX	98	105	25	18
t_{PZL}				98	105	25	18
t_{PHZ}	INH	COM or Yn	MAX	75	75	25	18
t_{PLZ}				75	75	25	18

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

4053

TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

Logic Diagram



FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	-	0.02	mA

SWITCHING CHARACTERISTICS

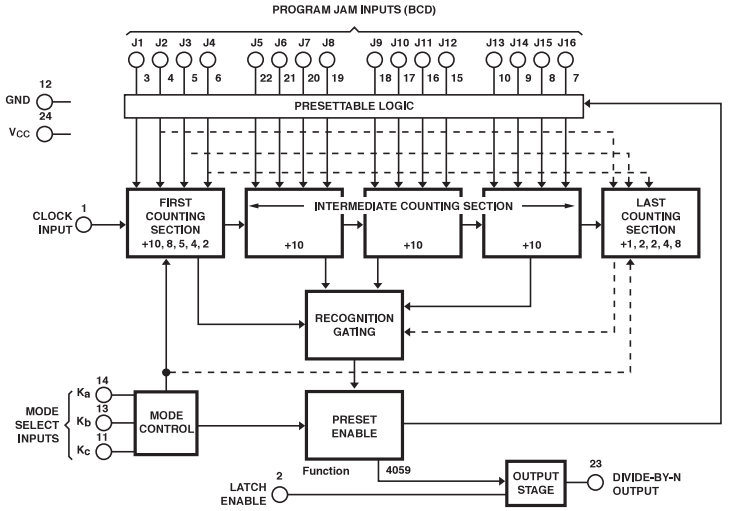
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	COM or Yn	Yn or COM	MAX	18	18	12	8
t_{PHL}				18	18	12	8
t_{PZH}	INH	COM or Yn	MAX	66	72	25	18
t_{PZL}				66	72	25	18
t_{PHZ}	INH	COM or Yn	MAX	63	66	25	18
t_{PLZ}				63	66	25	18

UNIT: ns

4059

CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER

Function Diagram



FUNCTION TABLE

MODE SELECT INPUT		
Ka	Kb	Kc
H	H	H
L	H	H
H	L	H
L	L	H
H	H	L
X	L	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
f_{max}	CP		MIN	18
t_w	CP		MIN	27
t_{su}	Kb, Kc to CP		MIN	22
t_{PLH}	CP	Q	MAX	60
t_{PHL}				60
t_{PLH}	LE	Q	MAX	53
t_{PHL}				53

UNIT fmax : MHz other : ns

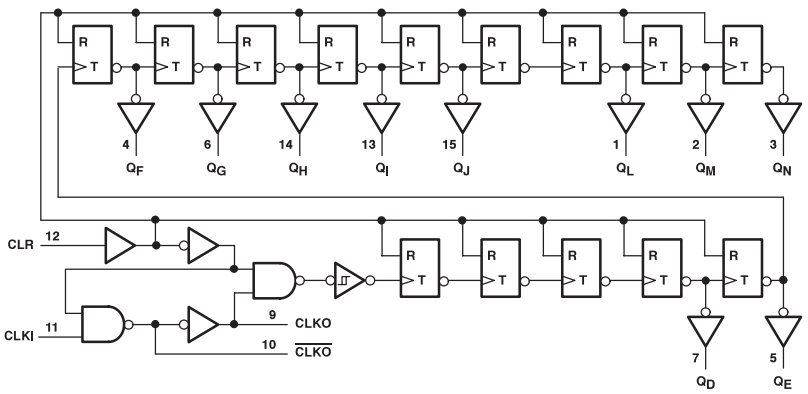
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4060

ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS

- Same Pinouts as CMOS4060
- Allow Design of Either RC or Crystal Oscillator Circuits
- V_{CC}: 2V to 6V

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS		
CLKI	CLR	Q_D to Q_N	CLKO	$\overline{CLKO}$
↑	L	No Change	↑	↓
↓	L	Advance to Next State	↓	↑
X	H	All Outputs are Low	L	H

OPERATING CONDITIONS

MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
MAX	0.08	0.16	0.16	mA
MAX	-4	-4	-4	mA
MAX	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
f_{max}			MIN	22	20	20
t_w	CLKI		MIN	23	24	24
	CLR high			23	24	38
t_{su}	CLR inactive before CLI		MIN	40	-	-
t_{PLH}	CLKI	Q_D	MAX	123	90	100
t_{PHL}				123	90	100
t_{PHL}	CLR	Any	MAX	35	53	66

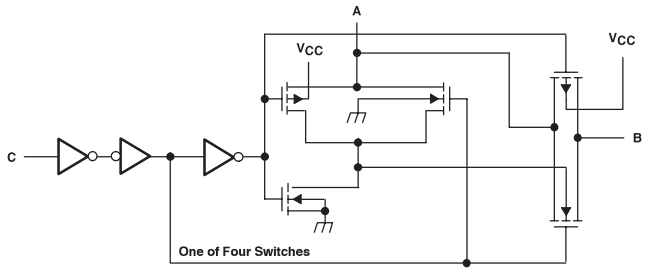
UNIT fmax : MHz other : ns

4066

QUADRUPLE BILATERAL SWITCHES

- Same Pinouts as CMOS4016, 4066
- Low On-State Impedance: 50-Ω TYP at V_{CC} = 6V
- Individual Switch Controls
- Extremely Low Input Current
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches

Logic Diagram



FUNCTION TABLE

INPUT (C)	SWITCH
L	OFF
H	ON

NOTE:
H = High Level
L = Low Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.02	0.04	0.04	-	0.02	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	A or B	B or A	MAX	15	18	18	12	8
t_{PHL}				15	18	18	12	8
t_{PZH}	C	A or B	MAX	45	30	36	22	16
t_{PZL}				45	30	36	22	16
t_{PHZ}	C	A or B	MAX	50	45	53	22	16
t_{PLZ}				50	45	53	22	16

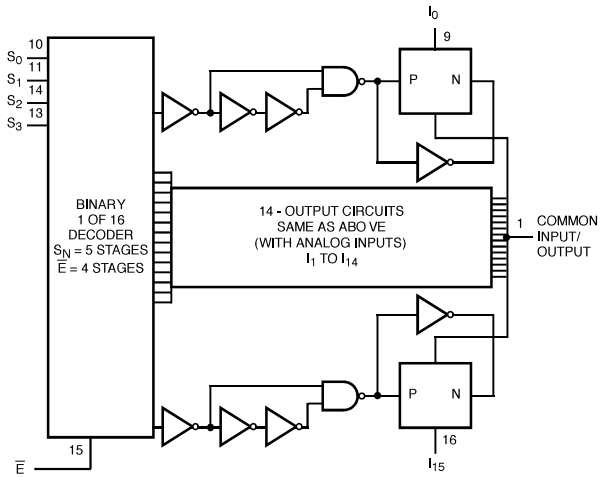
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4067

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

Function Diagram



FUNCTION TABLE

S0	S1	S2	S3	$\overline{E}$	SELECTED CHANNEL
X	X	X	X	X	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

NOTES:
H = High Level
L = Low Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{PLH}	Switch In	COMON I/O	MAX	22	22
t_{PHL}				22	22
t_{PZH}	$\overline{E}$	COMON I/O	MAX	83	90
t_{PZL}				83	90
t_{PZH}	Sn	COMON I/O	MAX	90	90
t_{PZL}				90	90
t_{PHZ}	$\overline{E}$	COMON I/O	MAX	83	83
t_{PLZ}				83	83
t_{PHZ}	Sn	COMON I/O	MAX	87	87
t_{PLZ}				87	87

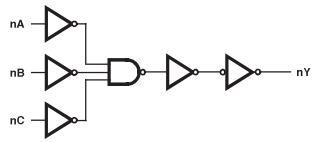
UNIT:ns

4075

TRIPLE 3-INPUT OR GATES

● Y = A + B + C

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

NOTES:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.02	0.04	0.04	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

SWITCHING CHARACTERISTICS

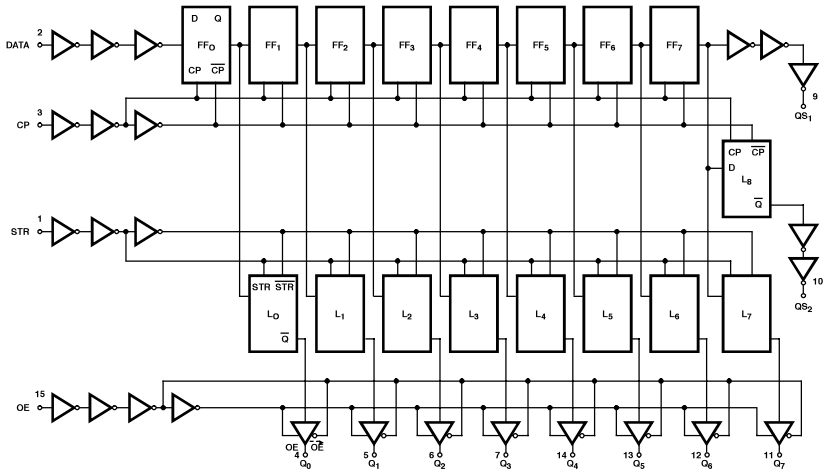
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A, B or C	Y	MAX	25	30	36
t_{PHL}	A, B or C	Y	MAX	25	30	36

UNIT:ns

4094

8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE

Logic Diagram



FUNCTION TABLE

INPUTS				PALALLEL OUTPUT		SERIAL OUTPUT	
CP	OE	STR	D	Q_0	Q_n	QS_1‡	QS_2
↑	L	X	X	Z	Z	Q'_6	NC
↓	L	X	X	Z	Z	NC	Q'_7
↑	H	L	X	NC	NC	Q'_6	NC
↑	H	H	L	L	Q_n-1	Q'_6	NC
↑	H	H	H	H	Q_n-1	Q'_6	NC
↓	H	H	H	NC	NC	NC	Q'_7

NOTES:
†. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, NC = No charge, Z = High Impedance Off-state. ↑ = Transition from Low to High Level, ↓ = Transition from High Low.
‡. At the positive clock edge the information in the seventh resister stage is transferred to the 8th register stage and QS_1 output.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OL}	MAX	4	4	mA
I_{OH}	MAX	-4	-4	mA

SWITCHING CHARACTERISTICS

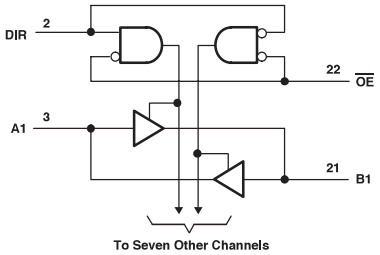
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_W	CP		MIN	24	24
t_{WH}	STR		MIN	24	24
t_{SU}	Data		MIN	15	15
	STR			30	30
t_H	Data		MIN	3	4
	STR			0	0
t_{PLH}	CP	QS1	MAX	45	-
t_{PHL}				45	-
t_{PLH}	CP	QS2	MAX	41	-
t_{PHL}				41	-
t_{PLH}	CP	Qn	MAX	59	-
t_{PHL}				59	-
t_{PLH}	STR	Qn	MAX	54	-
t_{PHL}				54	-
t_{PZH}	OE	Qn	MAX	53	-
t_{PZL}				53	-
t_{PLZ}	OE	Qn	MAX	38	-
t_{PHZ}				38	-

UNIT:ns

4245

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC	LVCC	UNIT
I_{CCA}	MAX	0.08	0.08	mA
I_{CCB}	MAX	0.05	0.08	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC	LVCC V_{CCB} 3.3V
t_{PLH}	A	B	MAX	6.3	7
t_{PHL}				6.7	7
t_{PLH}	B	A	MAX	6.1	6.2
t_{PHL}				5	5.3
t_{PZL}	$\overline{OE}$	A	MAX	9	9
t_{PZH}				8.1	8
t_{PZL}	$\overline{OE}$	B	MAX	8.8	10
t_{PZH}				9.8	10.2
t_{PLZ}	$\overline{OE}$	A	MAX	7	5.2
t_{PHZ}				5.8	5.2
t_{PLZ}	$\overline{OE}$	B	MAX	7.7	5.4
t_{PHZ}				7.8	7.4

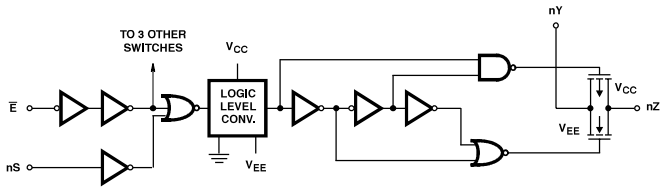
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4316

QUAD ANALOG SWITCH WITH LEVEL TRANSLATION

Logic Diagram



FUNCTION TABLE

INPUTS		
$\overline{E}$	S	SWITCH
L	L	OFF
L	H	ON
H	X	OFF

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA

SWITCHING CHARACTERISTICS

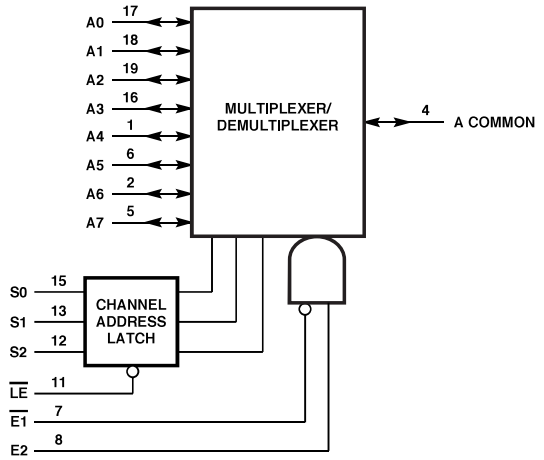
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{PLH}	Switch in	Switch out	MAX	18	18
t_{PHL}				18	18
t_{PZH}	$\overline{E}$	Z	MAX	62	66
t_{PZL}				62	85
t_{PZH}	nS	Z	MAX	53	60
t_{PZL}				53	75
t_{PLZ}	$\overline{E}$	Z	MAX	62	75
t_{PHZ}				62	-
t_{PLZ}	nS	Z	MAX	53	-
t_{PHZ}				53	66

UNIT:ns

4351

ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH

Logic Diagram



FUNCTION TABLE

INPUTS					"ON"† SWITCCHES
$\overline{E1}$	E2	S2	S1	S0	$\overline{LE}$ = H
L	H	L	L	L	A_0
L	H	L	L	H	A_1
L	H	L	H	L	A_2
L	H	L	H	H	A_3
L	H	H	L	L	A_4
L	H	H	L	H	A_5
L	H	H	H	L	A_6
L	H	H	H	H	A_7
H	L	X	X	X	None

NOTES:
† When LE is low S0-S2 data are latched and switches cannot change state.
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_W	$\overline{LE}$		MIN	30	28
t_{su}	Sn to $\overline{LE}$		MIN	-	-
t_H	Sn to $\overline{LE}$		MIN	5	5
t_{PLH}	Switch In	Switch Out	MAX	11	11
t_{PHL}				11	11
t_{PZH}	$\overline{E1}$, E2, $\overline{LE}$	Vos	MAX	90	113
t_{PZL}				90	113
t_{PZH}	Sn	Vos	MAX	90	113
t_{PZL}				90	113
t_{PLZ}	$\overline{E1}$	Vos	MAX	75	83
t_{PHZ}				75	83
t_{PLZ}	E2	Vos	MAX	75	90
t_{PHZ}				75	90
t_{PLZ}	$\overline{LE}$	Vos	MAX	83	90
t_{PHZ}				83	90
t_{PLH}	Sn	Vos	MAX	83	98
t_{PHL}				83	98

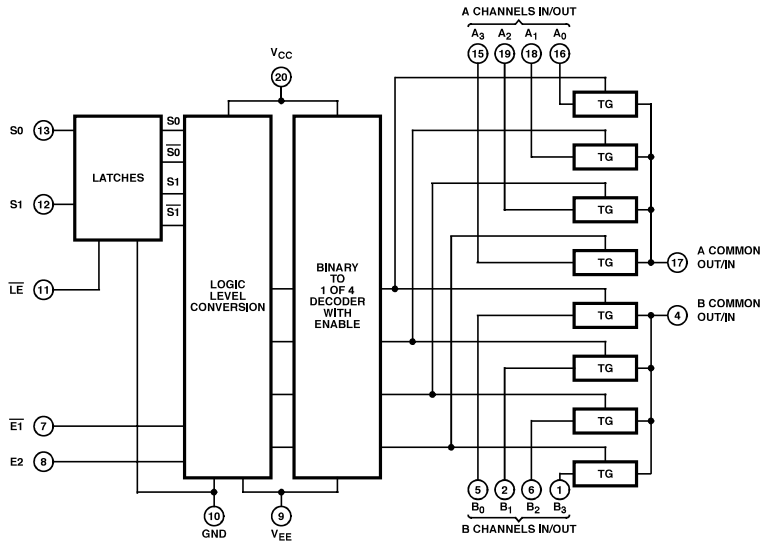
UNIT:ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4352

ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH

Function Diagram



FUNCTION TABLE

INPUTS				"ON"† SWITCCHES
$\overline{E1}$	E2	S1	S0	$\overline{LE}$ = H
L	H	L	L	A_0, B_0
L	H	L	H	A_1, B_1
L	H	H	L	A_2, B_2
L	H	H	H	A_3, B_3
H	L	X	X	None

NOTES:
† When LE is low S0-S2 data are latched and switches cannot change state.
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
tW	$\overline{LE}$		MIN	30
tsu	Sn to $\overline{LE}$		MIN	-
tH	Sn to $\overline{LE}$		MIN	5
tPLH	Switch In	Switch Out	MAX	11
tPHL				11
tPZH	$\overline{E1}$, E2, $\overline{LE}$	Vos	MAX	105
tPZL				105
tPZH	Sn	Vos	MAX	113
tPZL				113
tPLZ	$\overline{E1}$, E2, $\overline{LE}$	Vos	MAX	83
tPHZ				83

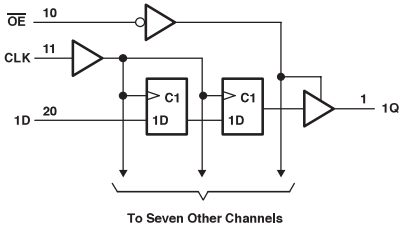
UNIT:ns

4374

OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STAE OUTPUTS

● 3-State Outputs Drive Bus Lines Directly

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I_{CC}	MAX	150	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
fmax			MIN	125
tw			MIN	4
tsu			MIN	4
th			MIN	1
tPLH	CLK	Q	MAX	8
tPHL				8
tPZH	$\overline{OE}$	Q	MAX	6
tPZL				8
tPHZ	$\overline{OE}$	Q	MAX	6.5
tPLZ				7

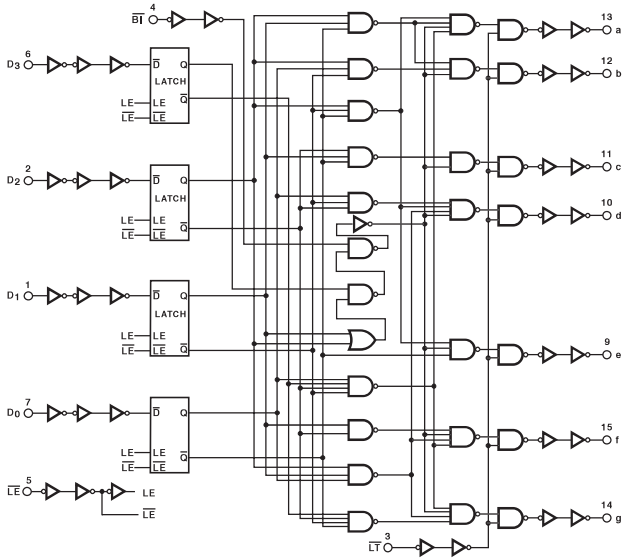
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4511

BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

Logic Diagram



FUNCTION TABLE

$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	H	L	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X								

NOTES:
X = Don't Care
Depends on BCD code previously applied when $\overline{LE}$ = L
Display is blank for all illegal input codes (BCD > HLLH).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-7.4	-7.4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

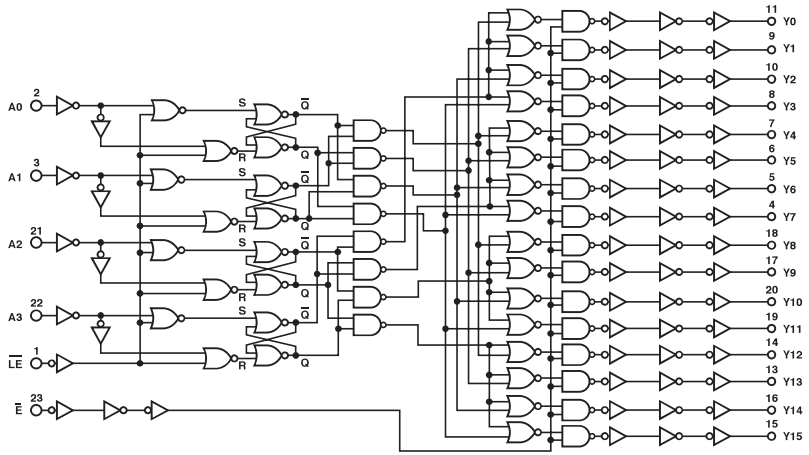
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_W	Latch Enable		MIN	20	20
t_{su}	Dn to $\overline{LE}$		MIN	20	20
t_H	Dn to $\overline{LE}$		MIN	3	5
t_{PLH}	Dn	a to g	MAX	75	75
t_{PHL}				75	75
t_{PLH}	$\overline{LE}$	a to g	MAX	68	68
t_{PHL}				68	68
t_{PLH}	$\overline{BI}$	a to g	MAX	55	55
t_{PHL}				55	55
t_{PLH}	$\overline{LT}$	a to g	MAX	40	41
t_{PHL}				40	41

UNIT:ns

4514

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
($\overline{LE}$ = H)

$\overline{E}$	DECODER INPUTS				ADDRESSED OUTPUT H
	A3	A2	A1	A0	
L	L	L	L	L	Y0
L	L	L	L	H	Y1
L	L	L	H	L	Y2
L	L	L	H	H	Y3
L	L	H	L	L	Y4
L	L	H	L	H	Y5
L	L	H	H	L	Y6
L	L	H	H	H	Y7
L	H	L	L	L	Y8
L	H	L	L	H	Y9
L	H	L	H	L	Y10
L	H	L	H	H	Y11
L	H	H	L	L	Y12
L	H	H	L	H	Y13
L	H	H	H	L	Y14
L	H	H	H	H	Y15
H	X	X	X	X	All outputs = L

H = high, L = low, X = don't care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.08	mA
I_{OH}	MAX	-4	-4	-6	mA
I_{OL}	MAX	4	4	6	mA

SWITCHING CHARACTERISTICS

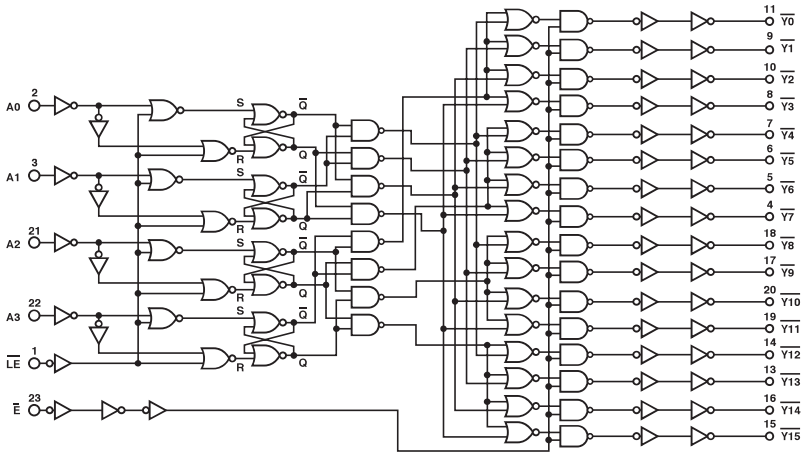
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_w	LE ($\overline{LE}$)		MIN	20	22	38
t_{su}	LE ($\overline{LE}$)		MIN	25	30	25
t_h	LE ($\overline{LE}$)		MIN	5	0	5
t_{PLH}	A, B, C, D (A1, 2, 3, 4)	Y	MAX	58	83	69
t_{PHL}				58	83	69
t_{PLH}	LE ($\overline{LE}$)	Y	MAX	58	68	63
t_{PHL}				58	68	63
t_{PLH}	$\overline{E}$	Y	MAX	44	53	50
t_{PHL}				44	53	50

UNIT:ns

4515

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
($\overline{LE}$ = H)

$\overline{E}$	DECODER INPUTS				ADDRESSED OUTPUT L
	A3	A2	A1	A0	
L	L	L	L	L	Y0
L	L	L	L	H	Y1
L	L	L	H	L	Y2
L	L	L	H	H	Y3
L	L	H	L	L	Y4
L	L	H	L	H	Y5
L	L	H	H	L	Y6
L	L	H	H	H	Y7
L	H	L	L	L	Y8
L	H	L	L	H	Y9
L	H	L	H	L	Y10
L	H	L	H	H	Y11
L	H	H	L	L	Y12
L	H	H	L	H	Y13
L	H	H	H	L	Y14
L	H	H	H	H	Y15
H	X	X	X	X	All outputs = H

H = high, L = low, X = don't care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.08	mA
I_{OH}	MAX	-4	-4	-6	mA
I_{OL}	MAX	4	4	6	mA

SWITCHING CHARACTERISTICS

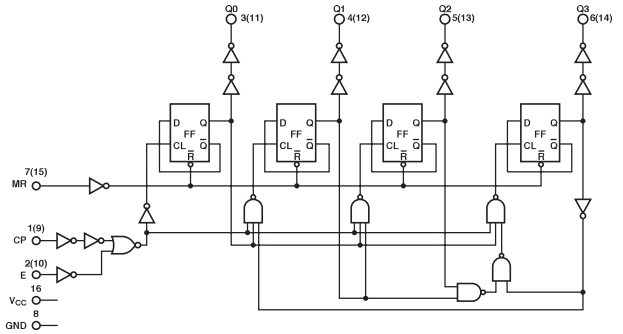
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_w	LE ($\overline{LE}$)		MIN	20	22	38
t_{su}	LE ($\overline{LE}$)		MIN	25	30	25
t_h	LE ($\overline{LE}$)		MIN	5	0	5
t_{PLH}	A, B, C, D (A1, 2, 3, 4)	$\overline{Y}$ (CD74HCT:Y)	MAX	58	83	69
t_{PHL}				58	83	69
t_{PLH}	$\overline{LE}$ (LE)	$\overline{Y}$ (CD74HCT:Y)	MAX	58	68	63
t_{PHL}				58	68	63
t_{PLH}	$\overline{G}$ ($\overline{E}$)	$\overline{Y}$ (CD74HCT:Y)	MAX	44	53	50
t_{PHL}				44	53	50

UNIT:ns

4518

DUAL SYNCHRONOUS COUNTERS

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT STATE
CP	E	MR	
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
H	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
L	X	H	Q_0 thru Q_3 = L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
fmax			MIN	20
tw	CP		MIN	24
	MR			30
tsu	Enable to CP		MIN	24
	CP to Enable			24
t_{PLH}	CP	Qn	MAX	72
t_{PHL}				72
t_{PLH}	Enable	Qn	MAX	72
t_{PHL}				72
t_{PLH}	MR	Qn	MAX	45
t_{PHL}				45

UNIT fmax : MHz other : ns